
Application Configurable System Cells

Description

Application Configurable System Cells (ACSCs), have been developed by Dialog Semiconductor for specific market segments. The System Cells consist of primary groups of function blocks which have been targeted at individual applications. The Design Engineer is able to utilize these blocks to build his system, and if necessary, have them customized by Dialog to exactly meet his requirements. Proven ASIC design and process technology mean that the circuits provide cost-effective and extremely reliable solutions to manufacturers within a variety of fields. Manufacturers benefit from a highly developed application-oriented product, with the added advantage that while it can be fully customized, both development times and risk factors can be significantly reduced. The concept allows the Design Engineer to build a system from proven high level circuit blocks, rather than designing at the standard cell or transistor level.

In any given market place the main participants are usually offering similar products. They differentiate themselves by offering variations on price, performance or functionality. One of the ways they can achieve differentiation is by developing ASICs which encapsulate these benefits. However, many of these potential users of ASICs may be concerned by what they perceive as risk or expense or long development time.

What is required by many system companies is a kind of 'instant ASIC' - the end result without the pain. With this in mind, Dialog has developed its ACSC strategy. ACSC is an attempt to distil the key

attributes of a given application into high level cells to which systems developers have access. By analyzing the common features of a market or application and then pre-developing the main blocks, most of the risk and much of the time element is removed from the equation. Individual systems developers can add as much or as little to the ACSC blocks as they wish. Indeed, the ACSC blocks can be used in standalone mode as discrete ICs, if preferred and, in fact, this may be the best way to start.

A system developer can design-in an ACSC like an ASSP and even go into production with it. As more is learned about the system, or if market feedback suggests it, changes may be required. With any sort of ASSP or standard product, changes are a major problem and can be lengthy and expensive. The ACSC, however, is designed to be flexible and modifying its performance or behaviour is intended to be straightforward. At heart, the ACSC is a technology demonstrator and adding circuitry around it is welcomed as a way of introducing more companies to the benefits of mixed signal ASICs

ACSCs developed by Dialog Semiconductor are targeted to vertical markets, for example, Satellite Communications, Video, Automotive, Security, and Utilities Metering applications.

Dialog has had extensive ASIC experience in the automotive field. Using this experience, Dialog has created a range of Major and Minor ACSC blocks to support our customers in specifying and designing ASICs for their automotive products.

In summary ACSCs are:

- A group of 'Expert Cells' targeted to a specific application
- A fully characterized mixed signal sub-system
- Usually available as packaged parts

Main benefits for the system user:

- Allows complete system development when used with field programmable parts
- Short development time
- Can be used to assess market
- Can be used for initial production
- Reduced technical risk

Ultrasonic Intrusion Detection Circuit

Description

This major ACSC function can either be used as a stand alone circuit, or as part of a larger custom circuit designed to suit specific application requirements. The DA5209 contains all the circuit functions necessary to implement an advanced low power, high sensitivity, ultrasonic movement detection system for automotive applications.

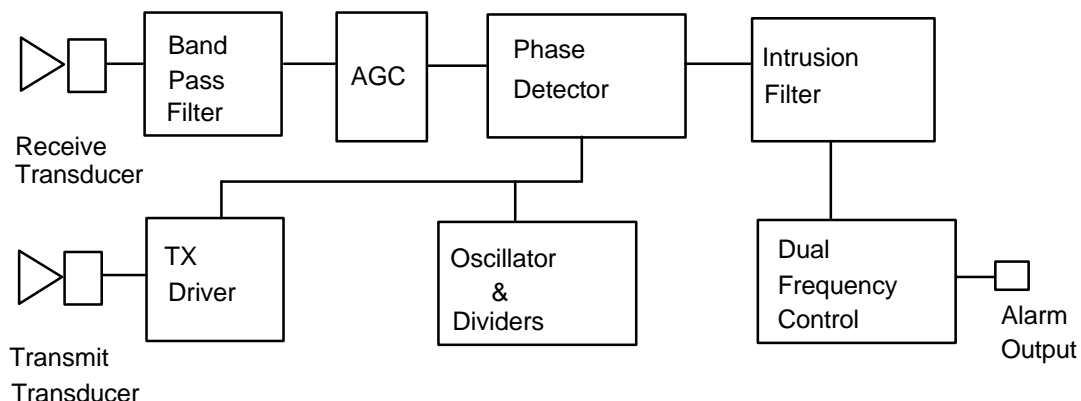
The large AGC range (80dB) of the DA5209 allows it to compensate automatically for the effects of temperature changes, vehicle volume and acoustic absorbency thus removing the need for adjustment at installation. The synchronous demodulator system which monitors both the magnitude and phase of the

return signal gives a significant improvement in sensitivity and noise rejection compared to more basic systems. The DA5209 operates at two slightly different signal frequencies under control of a timed sequencer which ensures that an intrusion has occurred at both frequencies before signalling an alarm. The technique avoids false alarms caused by signal cancellation occurring at one of the operating frequencies. The logic level alarm output and power down capability of the DA5209 enable it to be controlled by a microprocessor as part of comprehensive security systems. The DA5209 uses an advanced CMOS technology to enable this level of system integration to be achieved.

Features

- Complete stand alone system
- 80dB automatic gain control range
- Sensitive to both amplitude and phase disturbances
- Dual frequency operating mode
- 10mW active power dissipation
- Compact 20 pin SOIC package

Functional Block Diagram



High Precision Bridge Sensor Conditioning System

Description

This major ACSC is designed to directly connect to a monolithic bridge sensor and provide a temperature and sensor compensated analog output signal. Digital computation techniques enable a very high calibration resolution. The compensation data is stored in EEPROM which by means of a UART port can easily be calibrated after final assembly of the complete module.

The advantage of this concept is that a sensor with wide manufacturing tolerances can be used and electronically

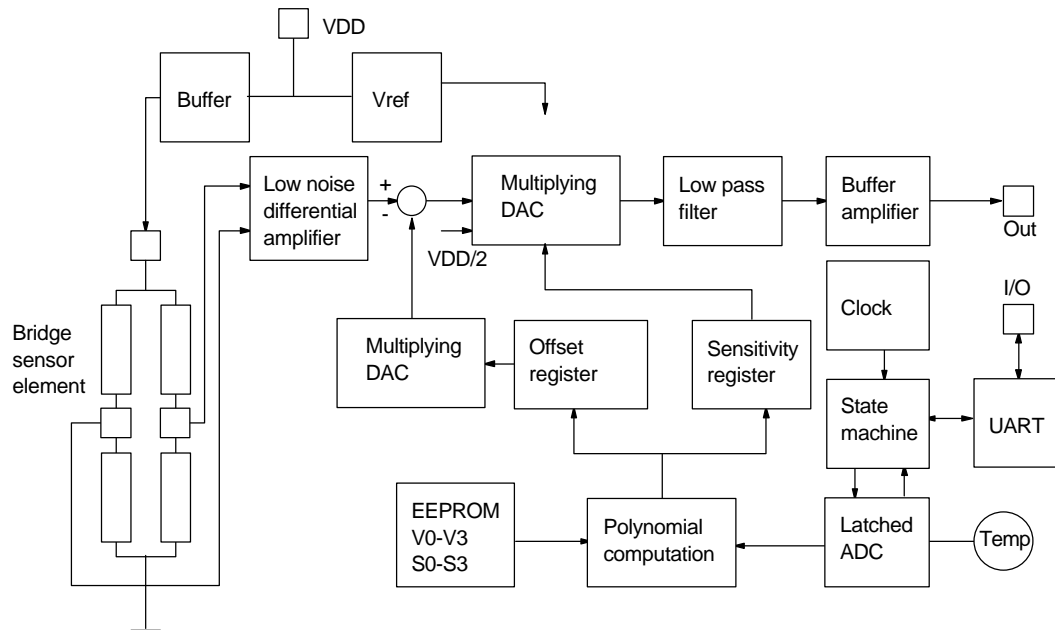
trimmed to a higher precision, thus avoiding expensive laser trimming. The EEPROM data storage also allows a system re-calibration if the sensor is changed.

During calibration the built-in temperature and external sensors are digitised and transmitted via the UART to the calibration system. This then calculates the required linearisation and offset parameters which are transmitted back to the cell. After testing this data it is written into EEPROM.

Features

- Works with low-cost sensors
- Directly connects to bridge acceleration sensor
- Low noise differential amplifier input stage
- Built-in 9 bit temperature sensor A/D
- 4th order digital polynomial computation for offset and gain compensation
- Temperature compensated offset DAC
- Gain error cancellation DAC
- EEPROM storage for compensation and error cancellation data
- UART Interface for system calibration
- -40°C to +120°C operation
- +5V single supply
- Requires no expensive laser trimming

Functional Block Diagram



Bridge Sensor Conditioning System

Description

This major ACSC is designed to directly connect to a monolithic bridge sensor and provide a temperature and sensor compensated analog output signal.

A 70 bit shift register is used to store calibration data of all programmable functions. After connecting the cell to a sensor the assembly can be calibrated. This is done by reading the uncalibrated values calculating the required compensation and then writing this data into

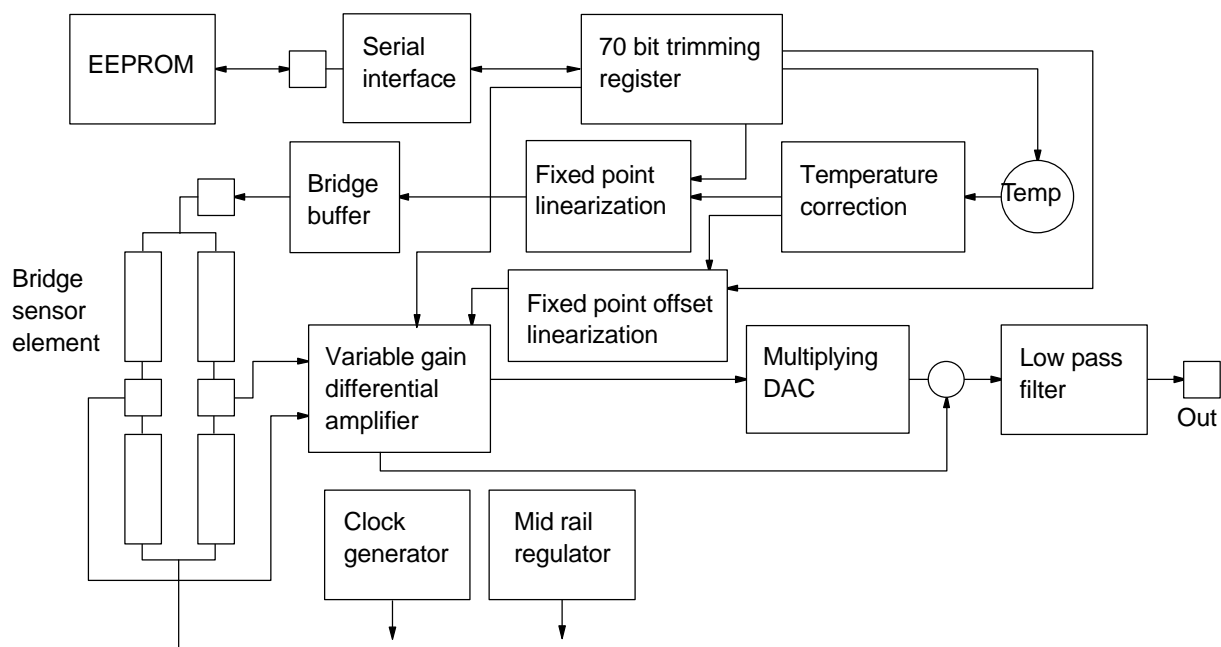
the shift register. When correct calibration has been achieved the data is written to EEPROM which is then used for normal operation.

The advantage of this concept is that a sensor with wide manufacturing tolerances can be used and electronically trimmed to a high degree of precision. The EEPROM data storage also means that a system can be re-calibrated should the sensor be changed.

Features

- Works with low-cost bridge sensors
- Built-in temperature sensor, and programmable temperature compensation
- Programmable fixed point sensor linearisation of both bridge drive and offset
- Programmable amplifier gain
- Programmed data stored in EEPROM
- Serial EEPROM interface
- -40°C to +120°C operation
- Single +5V supply
- Avoids expensive laser trimming

Functional Block Diagram



Temperature Sensor Conditioning Circuit

Description

This major ACSC generates an output voltage linearly proportional to temperature. It is primarily designed for monolithic temperature measurement applications. When combined with sensors having other physical properties (pressure, optical etc.) it can be used to correct their temperature sensitivity.

Most sensors require thermal corrective processing when used over a wide temperature range. The

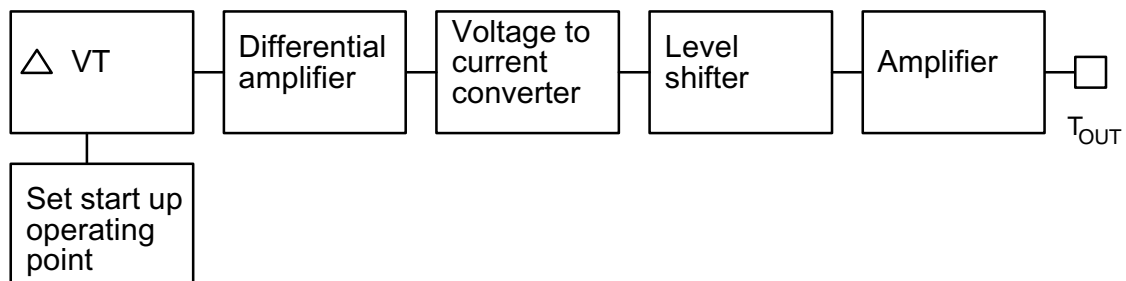
temperature proportional voltage generated by this cell can be used to compensate for this undesirable effect and allow a higher accuracy of overall measurement.

An integrated ΔV_T reference generates a temperature proportional voltage. The voltage is differentially amplified and fed to a series of current mirrors.

Features

- Linear $19.9\text{mV}/^\circ\text{C}$ scale factor
- 0.5°C accuracy at $+25^\circ\text{C}$
- Operating temperature range -40°C to $+95^\circ\text{C}$
- Low current consumption means minimal self-heating
- Single $+5\text{V}$ supply operation

Functional Block Diagram



Optical Positioning Sensor

Description

This major ACSC is designed primarily to remotely sense mechanical positioning in automotive engine management systems.

Eight photodiodes connect directly to current sources. Current mirror circuits, together with a common reference current, are externally adjustable. To give reliable operation the optical data is in gray code format. Schmitt trigger inputs are used to improve noise immunity before the data is clocked into a register.

A free-running gray counter turns the Pulse Width Modulator (PWM) on at a fixed counter state. This counter is then compared with the latched optical data. When both are equal the PWM output is switched off,

thus producing an output on-time proportional to the read gray code.

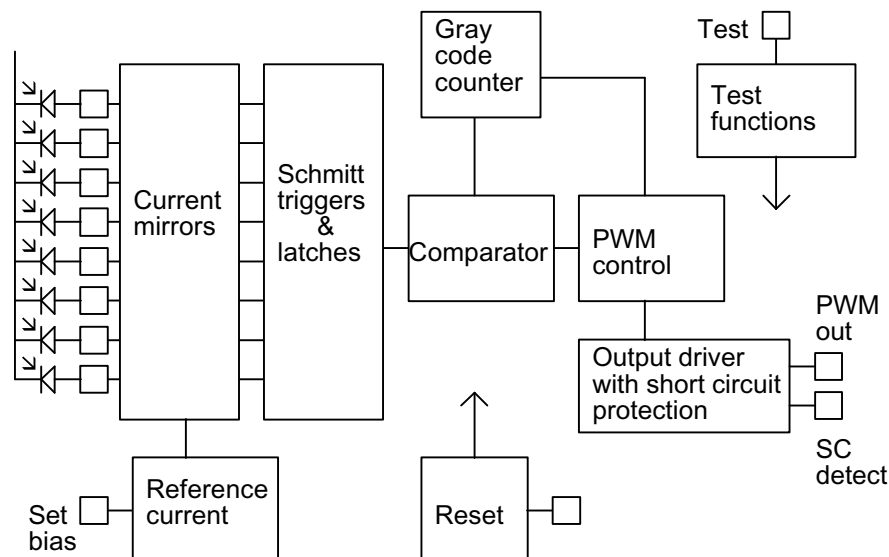
By modifying the counter states used together with different counter prescaling factors, it is easy to change both the duty cycle and cycle time of the PWM. The output driver stage incorporates a shunt resistor sensor which shuts the PWM output down upon detection of a short-circuit condition.

An integrated power-on reset ensures that the cell powers-up in a predefined state. It also reduces cable length from the central electronics to the remote sensor. Test mode circuitry enables the cell to be quickly checked for functionality without additional dedicated test outputs.

Features

- Converts optical gray code into PWM signal
- On-chip current biasing of sensor photodiodes
- Adjustable photodiode current
- Gray code ensures reliable operation
- Digital PWM allows easy modification of pulse widths
- Short circuit PWM output shuts driver down
- Single wire serial interface reduces system costs; test logic allows fast testing
- On-chip power-on reset
- Single +5V supply

Functional Block Diagram



PWM Motor Controller

Description

This major ACSC is designed to drive automotive DC universal motors. As a stand alone function it provides accurate speed control based on a variable reference clock input. Motor short circuit conditions are monitored and cause the device to shut-down thus avoiding electrical and mechanical damage. For safety critical applications an alarm output signals motor malfunction. Motor stalling conditions are also monitored and the motor power is proportionally reduced to avoid system damage.

The frequency comparator block compares the actual motor speed with the incoming reference clock. Based upon their relationship a pair of current sources are dynamically switched and integrated with a capacitor.

The capacitor charge is thus proportional to the actual motor speed. This variable threshold and a fixed sawtooth oscillator are then fed to a comparator which produces a pulse-width modulated output.

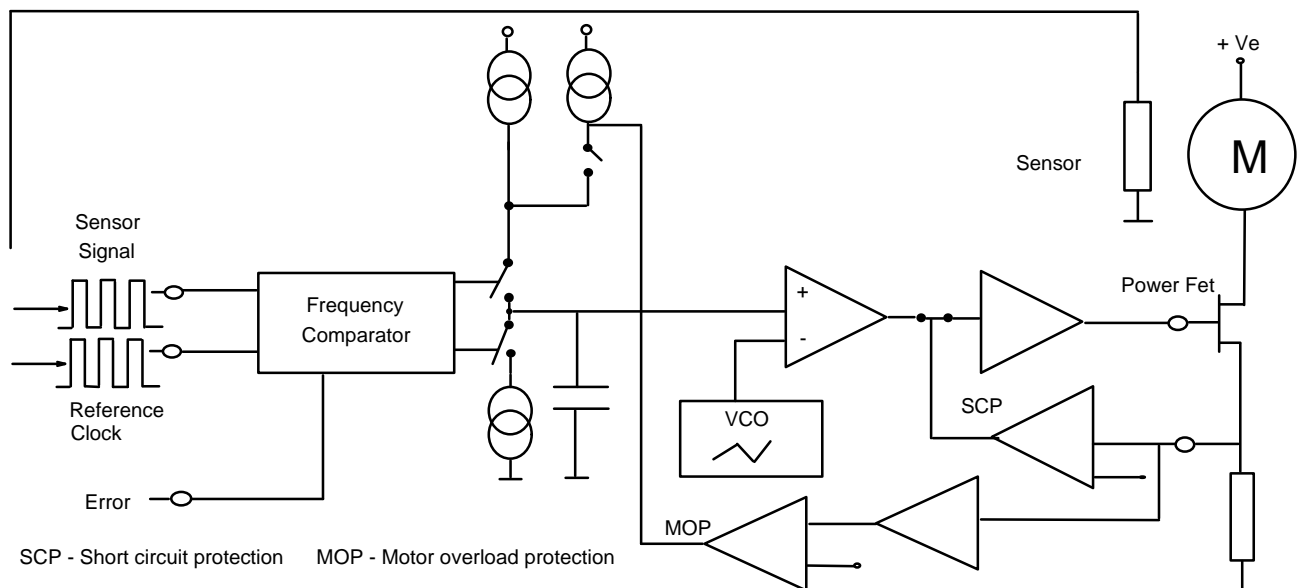
The voltage of an external motor shunt resistance is measured and if too high (motor short condition) shuts the driver stage down. To detect stalling conditions a second comparator is used, which changes the ratio of the current sources such that reduced power is applied to the motor.

Large differences between actual and set motor speeds generate an alarm output which can be used for diagnostic purposes.

Features

- Drives low cost universal motors
- Direct on-chip power FET driver
- Closed loop speed control
- Wide speed control range
- Motor short circuit shut-down
- Motor overload protection
- Digital diagnostic alarm output
- Single +5V supply

Functional Block Diagram



LCD Display Decoders / Drivers

Description

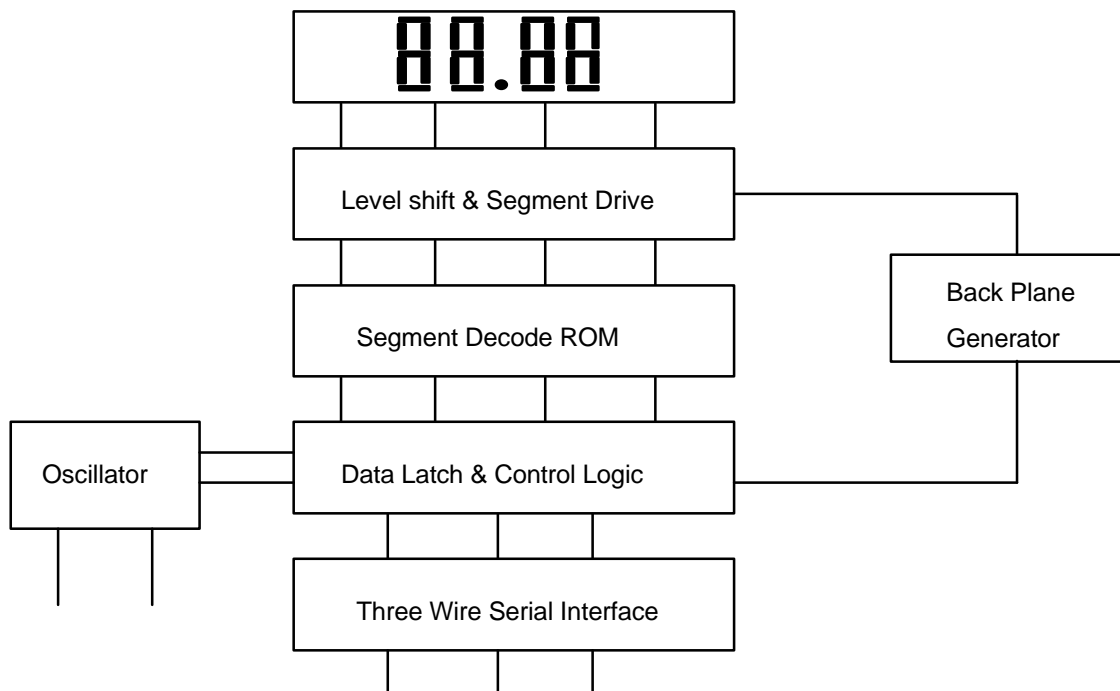
This major ACSC provides all the functions required to take in data either by serial interface or driven directly and decode the data to drive an LCD display. The ACSC can be fully customised to the number of segments per digit and the number of digits per display.

All backplane waveforms can be derived from the master oscillator. A power on reset function can also be provided.

Features

- Drives LCD directly
- 3-wire serial interface
- Backplane waveform generation
- Data latch and ROM decode
- Oscillator and frequency division
- Low power consumption

Functional Block Diagram



Multi-Function Timers

Description

Multifunction timers that can be customised to suit individual needs are available built from the minor ACSC functions detailed below.

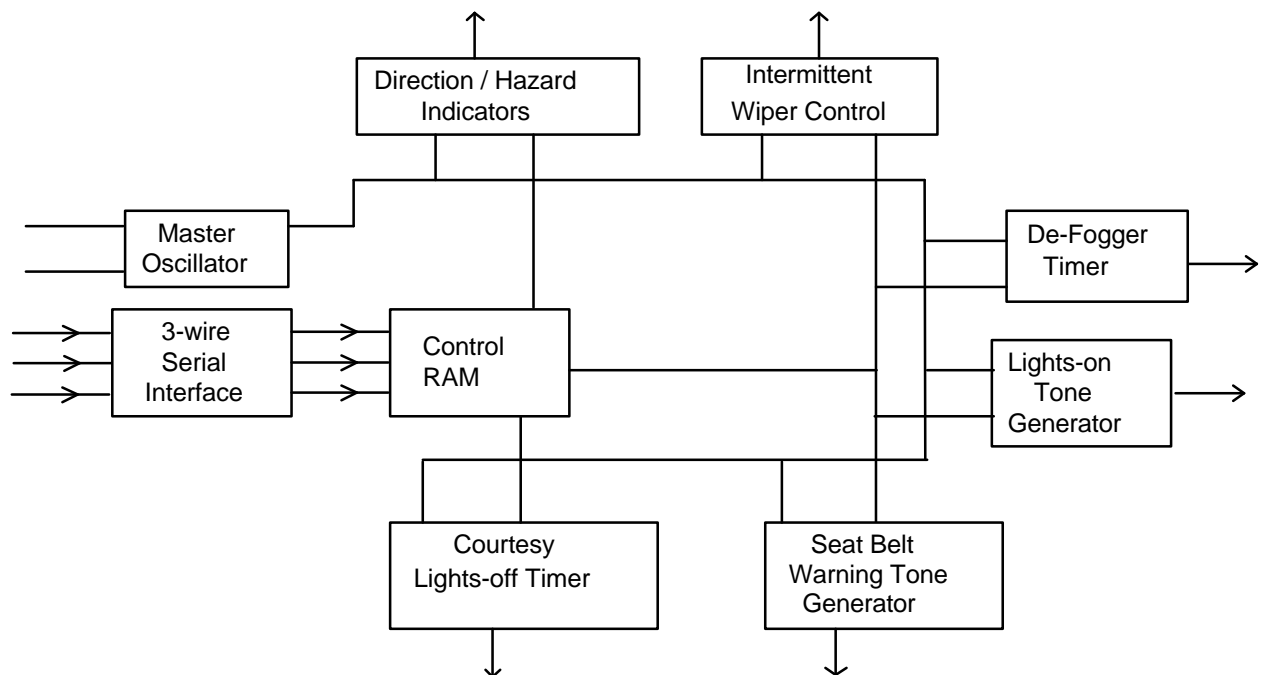
Programming can be by serial interface or by individual pins.

The two pin oscillator is intended for use with crystals and ceramic resonators. As an alternative, the ACSC can be driven from an external clock.

Features

- Multi-function timer suitable for all types of automotive application
- Fully programmable via a three wire serial interface
- Custom configurations available
- No external filter components required
- Single +5V supply
- Low power consumption

Functional Block Diagram



Siren Tone Generator Cell

Description

This major ACSC is a stand alone mixed analog/digital circuit which generates a number of pre-defined output waveforms for the purpose of driving the siren in a car-alarm system.

The chip produces a digital output whose frequency is determined by the output of an 8-bit binary-rate multiplier. A total of seven tones are produced. Five of these are fixed tones, and two are determined by the contents of an on-chip ROM. Tone selection is determined by the state of inputs SS0, SS1 and SS2.

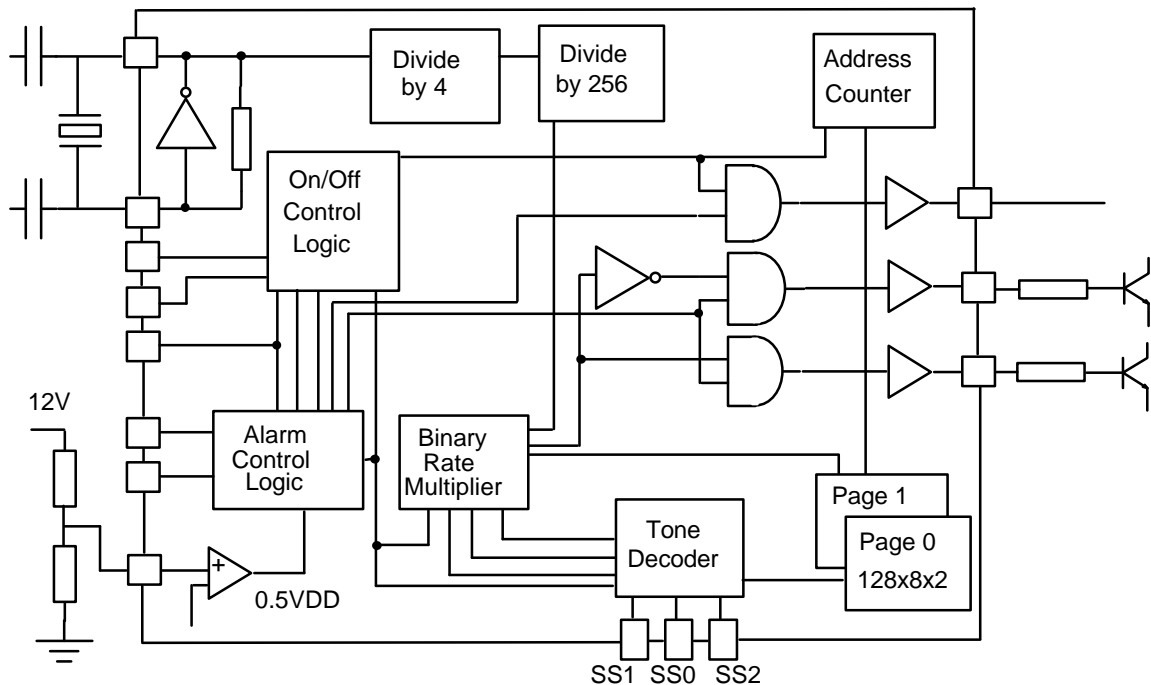
The selected tone is fed to two output buffers (true and complemented form) which provide the base-drive to two external npn devices which power the horn.

The chip is triggered into alarm mode either by a HIGH on the input pin, or by an internal comparator detecting the voltage on pin VBATT falling below $VDD/2$. This is intended to detect the removal of the car battery terminal. The alarm control logic pulses the alarm outputs on and off for a period determined by the state of the timer control inputs.

Features

- Complete stand alone system
- Generates up to 7 separate alarm sounds
- Meets international standards
- Mask ROM programmable
- Battery removal detection
- Few external components
- Low power
- Small size, compact SO16 package

Functional Block Diagram



Switched Capacitor Filters

Description

Cascaded biquad or RLC ladder sampled data filters may be provided using switched-capacitor structures with orders from 1 to > 20. For flexible, programmable and area-efficient filter structures, any number of 1st, 2nd and 3rd-order biquad sections may be cascaded and then simulated for effects of supply voltage, process and temperature variations prior to synthesis.

Dynamic range and frequency response can be extended by use of fully differential structures. Sin(x)/x, warping

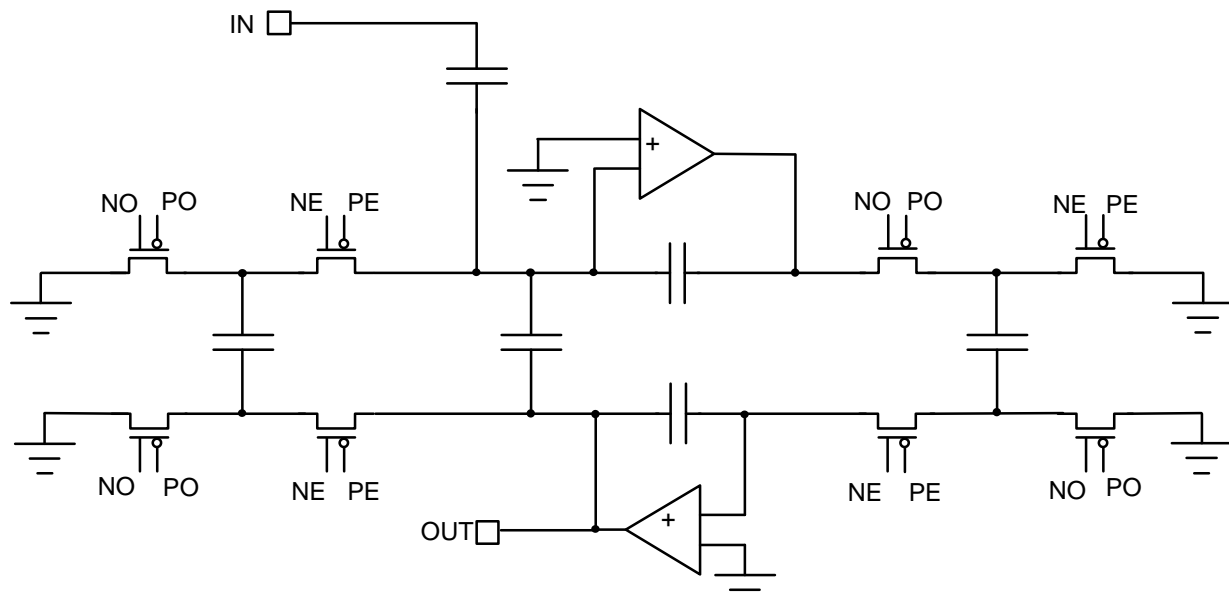
and aliasing effects are reduced by pre-warping the filter response and by use of 2nd or 3rd order continuous-time (active RC) filters which are included on chip. Filter sensitivity is reduced by use of ladder, rather than cascaded biquad, SCF structures.

Non-overlapping clock phases required by the SC switches are generated using standard cell circuits.

Features

- Handles signal frequencies from <0.1Hz to >250kHz
- Uses on-chip anti-aliasing filters
- No external (off-chip) components required
- Either ±5V, +5V or +3V supplies may be catered for
- Clock phases generated on-chip from just one external (stable) clock
- Gains and pole positions accurate to within 0.05%
- Filters, integrators, differentiators, rectifiers and comparators may be realised

Functional Block Diagram (2nd Order Biquad)



Digital Filters

Description

When reproducible, accurate and/or programmable filtering is required in a single-chip solution a digital filter should be considered. DSP solutions can be provided to a wide range of requirements. These may be used in conjunction with other mixed signal cells such as amplifiers, Continuous Time (CT) filters, ADCs and DACs as exemplified in the schematic below. Using Dialog's DSP Design and Synthesis tools, the filter is designed, optimised and simulated at gate/block level for a bit-true realisation.

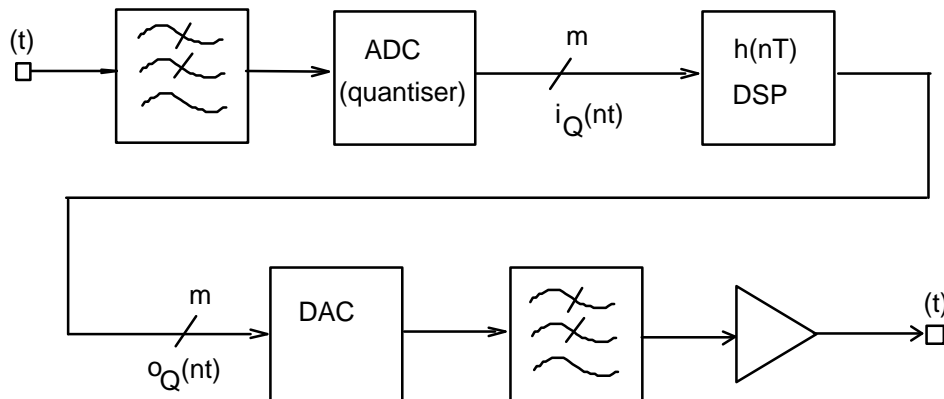
Finite word-length analysis, limit-cycle investigations and noise analyses are carried out prior to transfer for ASIC routing tools for area-efficient synthesis. VHDL may also be used for design entry, simulation or logic synthesis.

Code is generated for use in prototyping (FPGA or DSP board) when hardware is required prior to silicon availability.

Features

- Filters of virtually any order may be realised
- Supply voltages of 2.7-5.5V catered for
- Supported by prototyping
- Operation may be programmable
- FIR or IIR
- Adaptive filters
- May be used in conjunction with on-chip data-converters for analog-in / analog-out integration

Functional Block Diagram



CT Filters (Trimmable)

Description

Continuous-time (CT) Filters may be realised in an integrated circuit and this provides a useful function block for anti-aliasing, smoothing, reconstruction, etc. This produces a small-area silicon solution (see datasheet for CT Filters (Anti-alias)) but when accurate filter characteristics or higher order filters are required, an alternative technique (such as mosfet-C or trimmable-pole) must be employed.

The circuit below shows a fifth-order Butterworth low-pass filter using on-chip (polyfuse) trimming of the pole frequencies to ensure better than 10% accuracy in

positioning. To maximise the dynamic range, reduce the effect of switching spikes elsewhere in the IC system, and reduce common mode interference, a fully differential structure is shown.

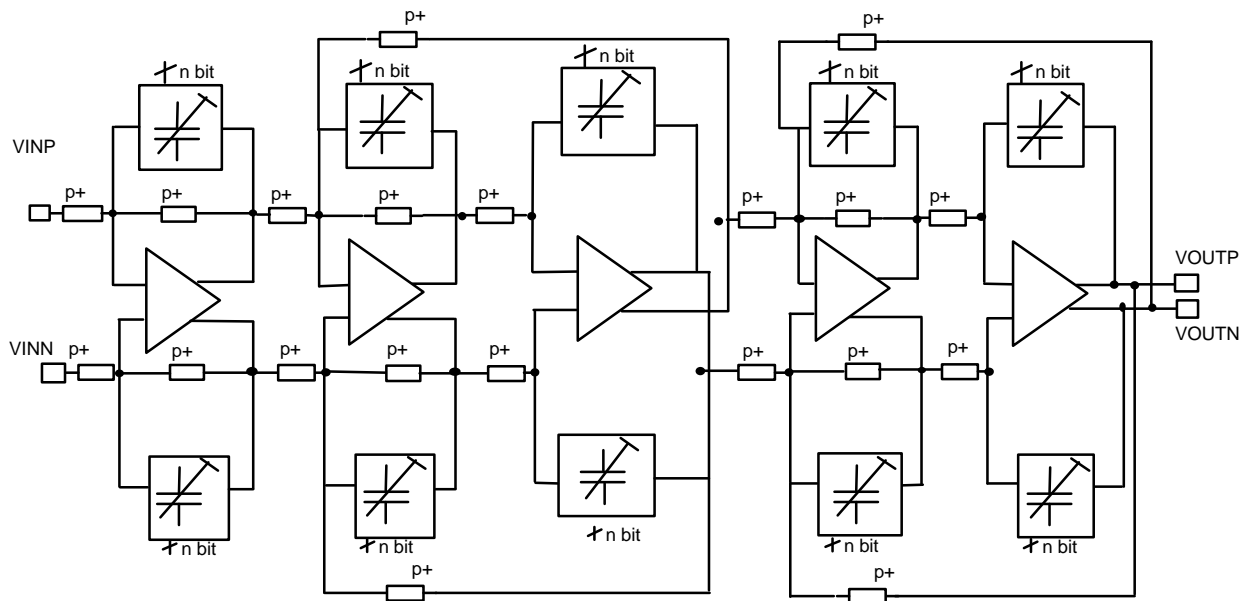
For any chosen filter structure the pole Q is determined by a single resistor ratio so that once all the pole frequencies have been adjusted by a common increment, the pole Q's of individual filter stages can be adjusted to control group delay.

Filters realised in this way may be trimmed during wafer sort and after packaging.

Features

- Low noise
- 10% accuracy cut-off (trimmed by polyfuse)
- Frequencies from 1kHz to 5Mhz
- Can be powered down
- High dynamic range (up to 100dB)
- Area efficient
- No external components required
- No clock or PLL required

Functional Block Diagram



CT Filters (Anti-Alias)

Description

Continuous Time (CT) filters are realised on CMOS integrated circuits by using various resistor structures (e.g. n-well or p-well) in combination with suitable capacitors (e.g. poly1/poly2) and opamps. This form of CT Filter will exhibit pole position uncertainty because of process spreads and values but this variability of "cut-off frequency" of up to 50% can be tolerated in certain applications and designed-in for anti-alias/reconstruction filters used in conjunction with sampled-data signals.

The usual form of integrated CT Filter is 2nd order (high-pass or low-pass) employing the "Sallen & Key" topology but higher orders may be realised with due consideration given to distortion, cut-off frequency and Q.

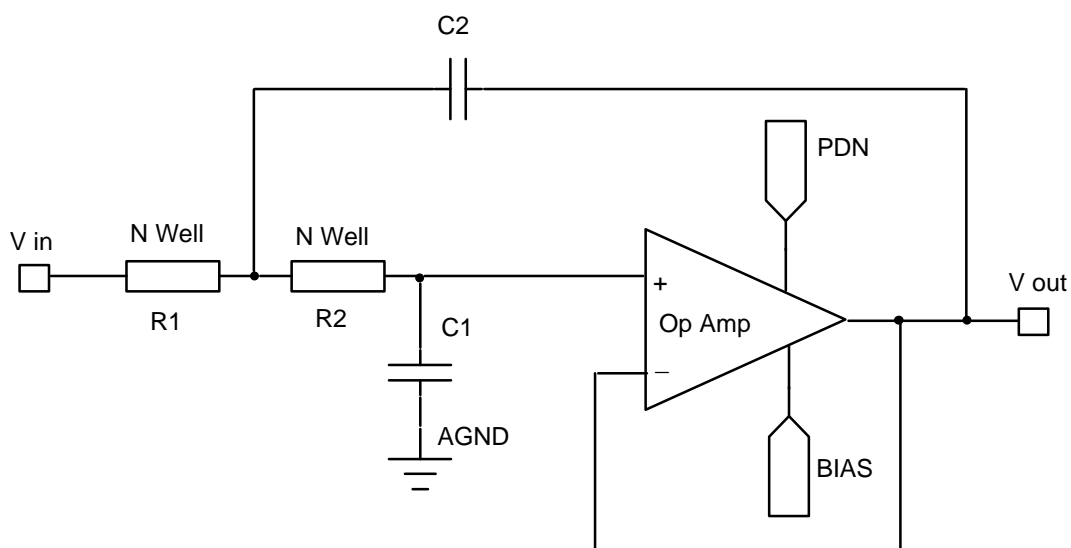
Different resistor and capacitor structures may be chosen (depending on the CMOS process used) for a trade-off on size/absolute accuracy/linearity/frequency. A particular benefit of this type of integrated filter is good noise performance.

For CT Filters requiring accurate pole locations methods such as mosfet-C, trimmable R/C, or external R and/or C are available (see CT Filters (Trimmable) datasheet).

Features

- Low noise
- May be powered down
- Wide range of supply voltages
- Compact structures (small silicon area)
- For anti-aliasing or reconstruction filter
- Wide range of cut-off frequencies (1kHz to 5Mhz)
- Accurate if used in conjunction with external components or trimming
- Efficient silicon area

Functional Block Diagram



Linear Voltage Controlled Oscillator (VCO)

Description

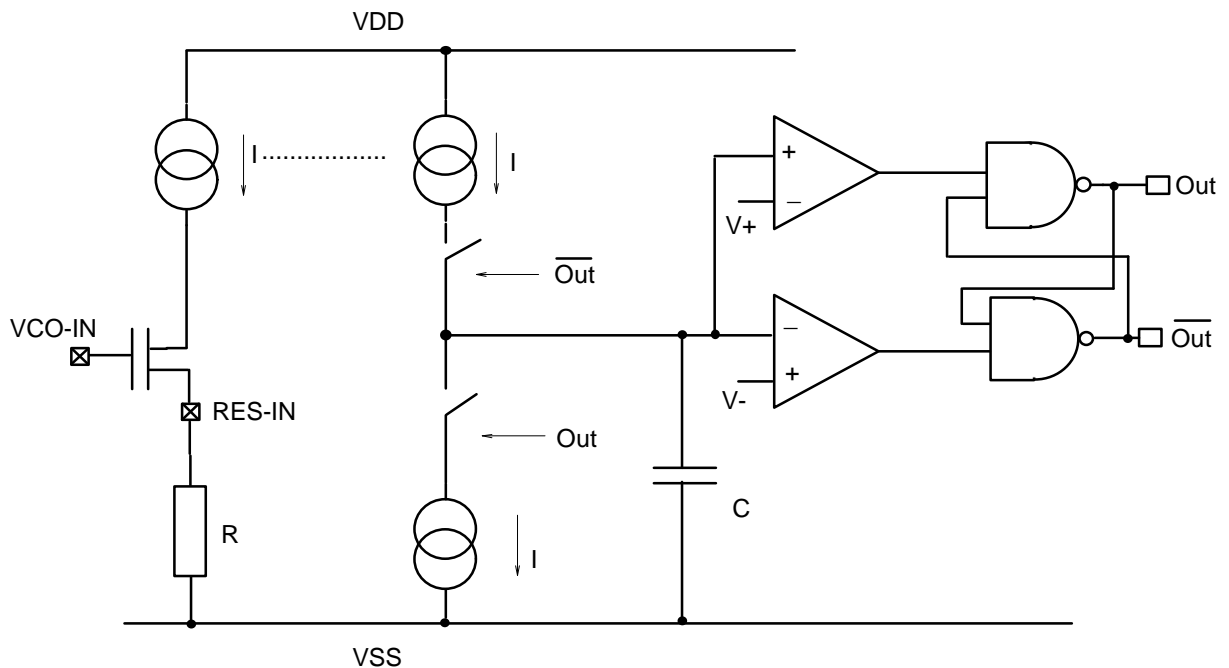
This minor ACSC produces an output signal whose frequency is determined by the voltage at the VCO-IN input, and the resistor connected to the RES-IN input. The resistor and the input voltage define a current within the VCO that is used to charge and discharge an internal capacitor between two threshold voltages.

When used in conjunction with a standard phase/frequency comparator and loop filter components, a phase-locked loop (PLL) can be formed to generate a wide range of frequencies. The use of ratio N/M division can additionally provide a direct frequency synthesis function.

Features

- Low power (100uA or less)
- Programmable frequency range
- Applications include direct frequency synthesis
- Typical frequencies ~ 1kHz to 5MHz

Functional Block Diagram



Oscillator for Ceramic Resonators

Description

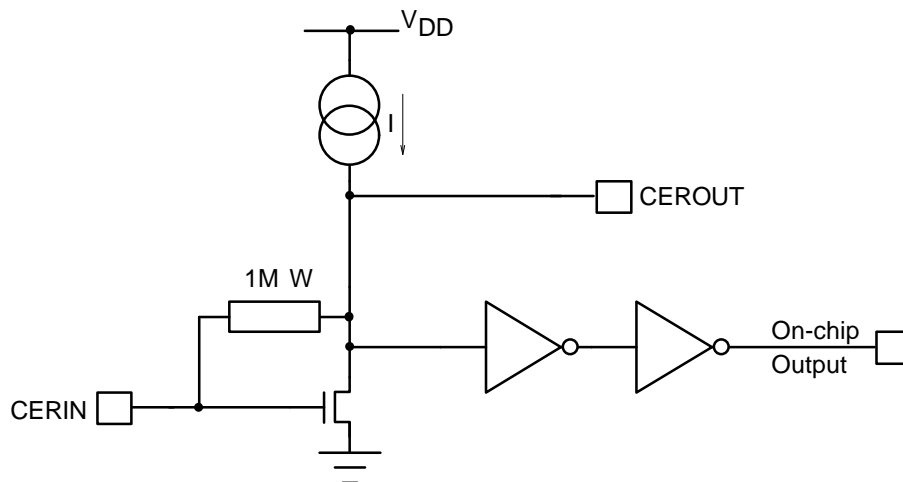
This minor ACSC is a 2-pin oscillator based on a single-stage class A amplifier. This minimises the output voltage swing and therefore current/power dissipation.

An internal $1M\Omega$ (nom.) feedback resistor is provided, saving an external component. The oscillator cell, when used with a resonator with integral load capacitors provides a low-cost and compact stable timebase for many applications.

Features

- 2 pin oscillator, well suited for use with ceramic resonators
- Frequency range 0.5MHz to 4MHz
- Feedback resistor ($1M\Omega$) on-chip saves external components
- Operating current $200\mu A$ or less at 4MHz

Functional Block Diagram



Crystal Oscillator

Description

This minor ACSC function is a 2-pin oscillator intended for use with crystals and ceramic resonators.

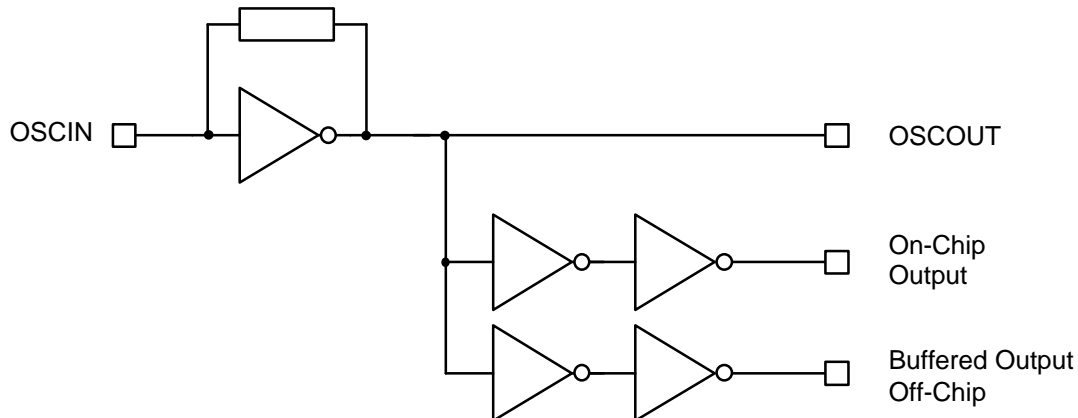
An internal $1\text{ M}\Omega$ (nom.) feedback resistor saves an external component and simplifies board layout.

The output of the oscillator can be buffered and brought off-chip through a suitably-sized driver to provide a system clock to the rest of the board.

Features

- 2 pin oscillator, suited to use with ceramic resonators from 6 to 12MHz, or crystals up to 20MHz
- Internal $1\text{ M}\Omega$ (nom.) feedback resistor saves external component
- Operating current with 12MHz resonator typically 1.5mA

Functional Block Diagram



RC Oscillator

Description

This minor ACSC function is a 1-pin relaxation oscillator. Frequency variations for $f < 1\text{kHz}$ is primarily set by external components.

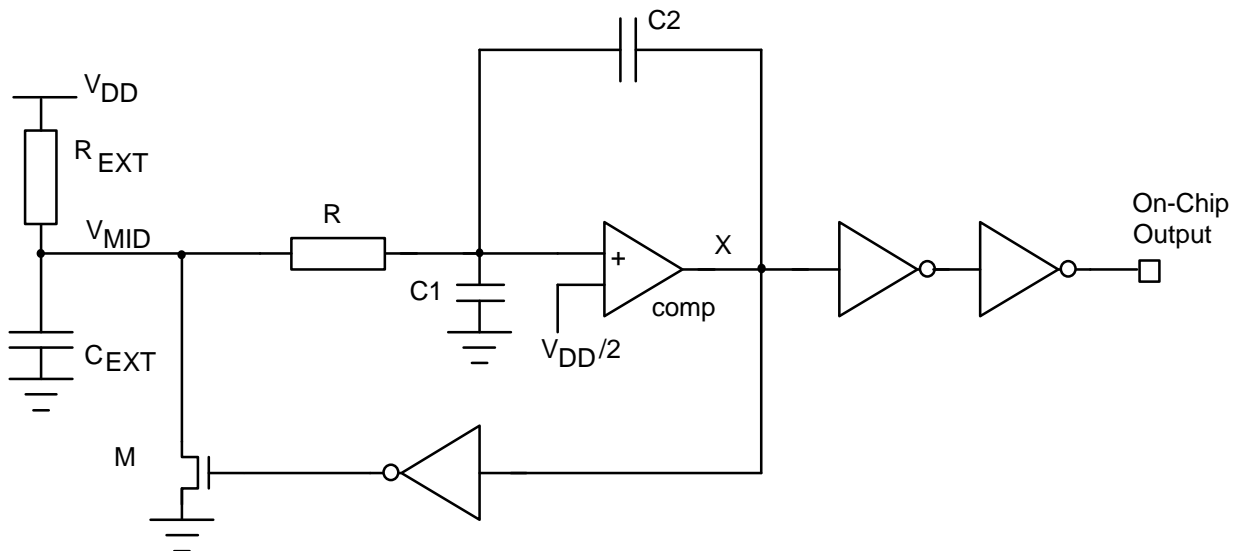
$$t_{\text{osc}} = 0.693 (R_{\text{EXT}} C_{\text{EXT}} + 6\mu\text{s})$$

As V_{MID} crosses $V_{\text{DD}}/2$, comp output x goes high, switching on the pull down device M, for time $RC1$, completely discharging V_{MID} to 0V. M then switches off, causing V_{MID} to charge up towards V_{DD} again.

Features

- Single-pin oscillator, suitable for generating low-frequency clocks ($< 1\text{kHz}$)
- Frequency determined by external R and C
- Low operating current (for $R = 1\text{M}\Omega$, $C = 4.7\text{nF}$, $f = 310\text{Hz}$, $I_{\text{DD}} = 35\mu\text{A}$)

Functional Block Diagram



Low Impedance Driver

Description

This minor ACSC function is an audio frequency 3 stage buffer with $\pm 12\text{mA}$ output current capability designed specifically to drive low impedance loads such as dynamic transducers.

A double folded cascode input stage provides high front end gain for the intermediate common mode gain stage.

Complementary source followers provide gate drive to the output MOSFETs whilst minimising crossover distortion normally associated with class B output stages.

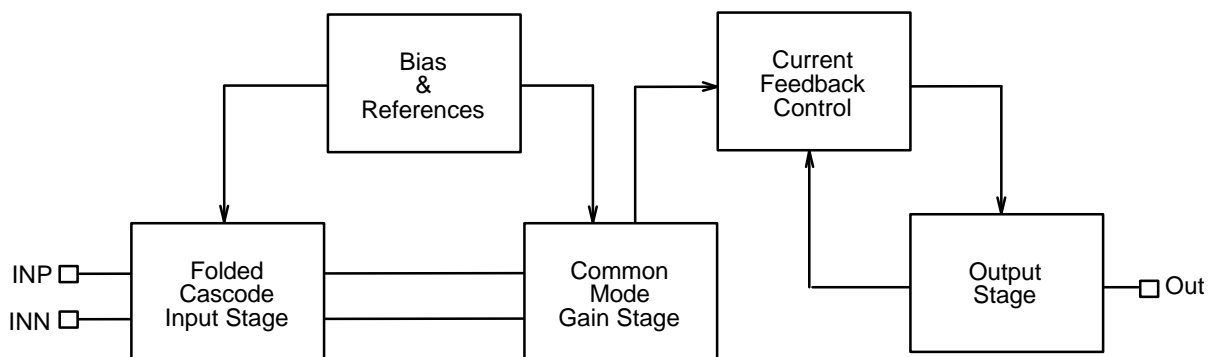
Supply current is minimised by use of a quiescent current feedback control block which monitors the output device current and adjusts the drive to the source followers whilst maintaining stability.

The buffer is internally compensated and will drive capacitive loads up to 100pF rail to rail.

Features

- High current drive buffer provides 4Vpp output into 180 Ω with <0.5% THD ($V_{dd} \geq 4.8\text{V}$)
- Three stage design with current feedback control only takes 300 μA typical quiescent current
- 105dB open loop gain 200kHz unity gain bandwidth 90dB PSRR at 1kHz
- Pair of drivers may be used to drive load differentially

Functional Block Diagram



Low Noise Amplifier

Description

This minor ACSC function is a MOSFET input low noise amplifier with rail to rail output buffer, designed for applications requiring a high input impedance.

The front end consists of P-channel cascoded input devices which have been sized with their loads to provide low flicker noise ($1/f$ knee $<100\text{Hz}$).

Noise performance is suitable for critical applications; equivalent input referred noise from 50Hz - 3.4kHz is $1.6\mu\text{Vrms}$. Supply rejection exceeds 80dB across this band.

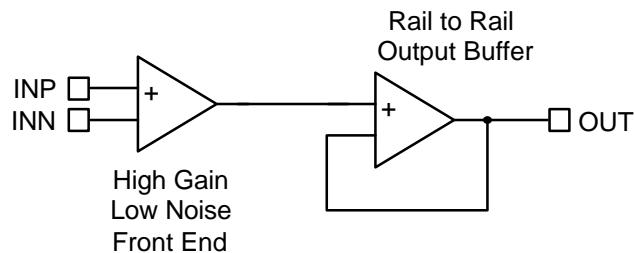
Thermal noise is $<25\text{nV/Hz}^{1/2}$.

The output buffer provides low distortion ($<0.05\%$ THD) for $\pm 2.0\text{V}$ in to $10\text{k}\Omega/50\text{pF}$.

Features

- High input impedance, low noise amplifier
- Configured with gain for optimum low noise path
- Cascoded front end provides $>80\text{dB}$ PSRR up to 4kHz
- Supply current of $320\mu\text{A}$, $V_{\text{dd}}(\text{min})$ of 4.8V
- Open loop gain of 120dB, Unity Gain BW of 1MHz

Functional Block Diagram



Rail to Rail Amplifier

Description

This minor ACSC function is an internally compensated, unity gain stable buffer.

True rail to rail operation is achieved by twin input stages with a low-gm, low distortion input crossover stage.

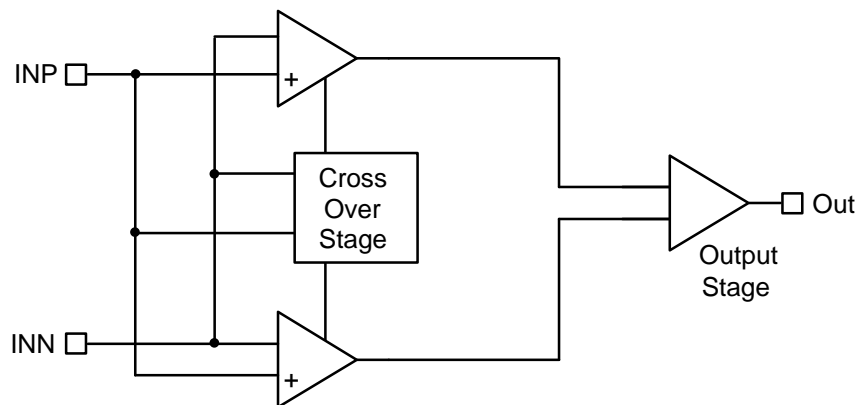
The pseudo push-pull output stage provides low distortion with low (250 μ A) quiescent current.

Open loop gain and bandwidth are 96 dB, 1MHz respectively.

Features

- Dual input stage gives rail to rail input common mode range
- Rail to rail output for capacitive loads up to 50pF
- $\pm 1.9V$ into 10k Ω load; $\pm 0.7V$ into 2.5k Ω load (Vdd=4.8V, THD \leq 0.03%)
- Low supply voltage (2.7V) capability with rail to rail operation
- Higher output drive variant available ($\pm 2.1V_{pk}$ into 1K Ω , Vdd=4.8V, 500 μ A quiescent)

Functional Block Diagram



Mid-Reference Buffer

Description

This minor ACSC function is a unity gain analog ground buffer with complementary source follower outputs, providing matched output current capability.

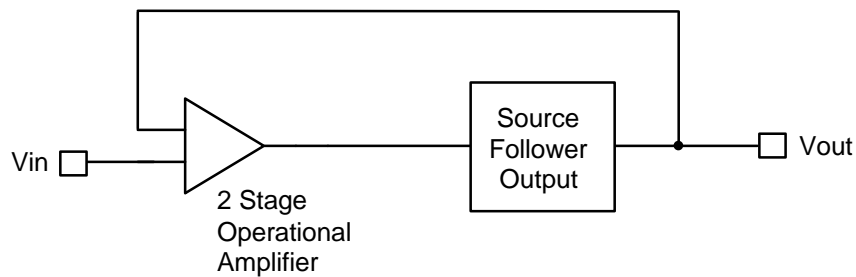
Internally compensated to remain stable for capacitive loads up to 100pF.

Nominal open loop gain and bandwidth is >75 dB and 600KHz respectively.

Features

- Less than 0.1% load regulation at 2.5V for 2.4mA output current
- Equal output current source and sink capability
- Low quiescent current 250 μ A
- High input resistance from MOSFET inputs

Functional Block Diagram



Driver Amplifier

Description

This minor ACSC is an internally compensated, unity gain stable buffer.

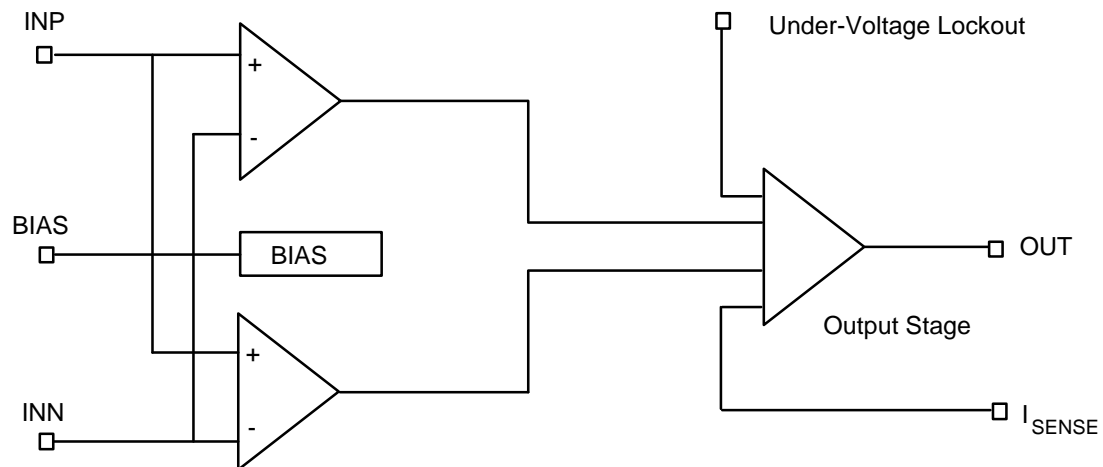
Complementary input stages provide rail to rail input common mode range. A pseudo push pull output stage provides low distortion with low quiescent current.

Higher output drive variants are available as defined by the required specification.

Features

- Operating Temp Range: -40 to +125 deg C
- Operating Voltage Range: -4.5 to 11V
- Open loop gain and bandwidth are 90db and 250kHz respectively
- Drives $\pm 5V$ into 2k load ($V_{DD}=11V$); Rail to rail output for capacitive loads up to 100pf
- Under voltage lockout and short circuit protection circuitry compatible

Functional Block Diagram



Driver Amplifier

Description

This minor ACSC is an internally compensated, unity gain stable buffer.

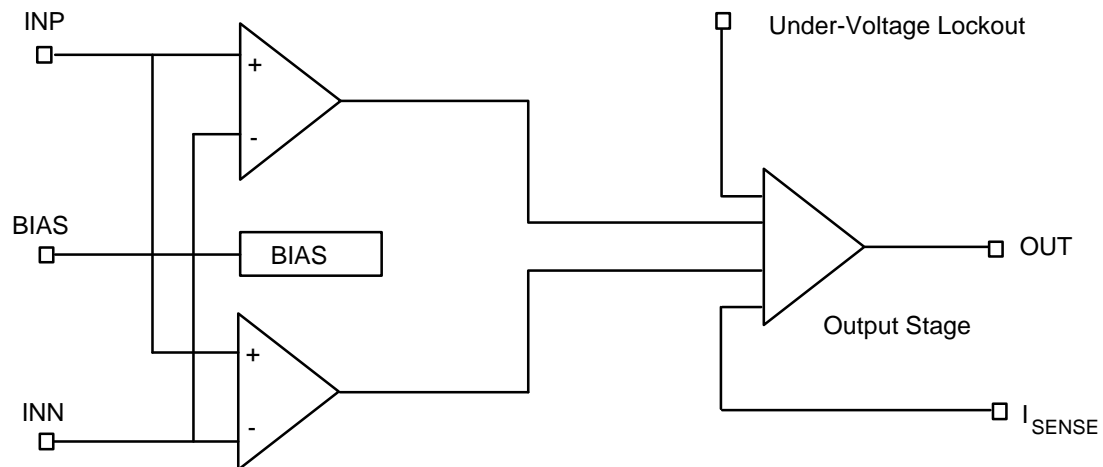
Complementary input stages provide rail to rail input common mode range. A pseudo push pull output stage provides low distortion with low quiescent current.

Higher output drive variants are available as defined by the required specification.

Features

- Operating Temp Range: -40 to +125 deg C
- Operating Voltage Range: -4.5 to 11V
- Open loop gain and bandwidth are 90db and 250kHz respectively
- Drives $\pm 5V$ into 2k load ($V_{DD}=11V$); Rail to rail output for capacitive loads up to 100pf
- Under voltage lockout and short circuit protection circuitry compatible

Functional Block Diagram



General Purpose DAC

Description

This minor ACSC function is a medium speed CMOS 8 bit resistor sub ranging DAC with buffered voltage output.

Depending on the input code a 16 element sub ranging resistor (SubR) is connected across two adjacent taps of a 16 element tapped resistor. The four major bits determine the position of the SubR resistor on the

tapped resistor whilst the minor bits decode the sub ranging resistor itself.

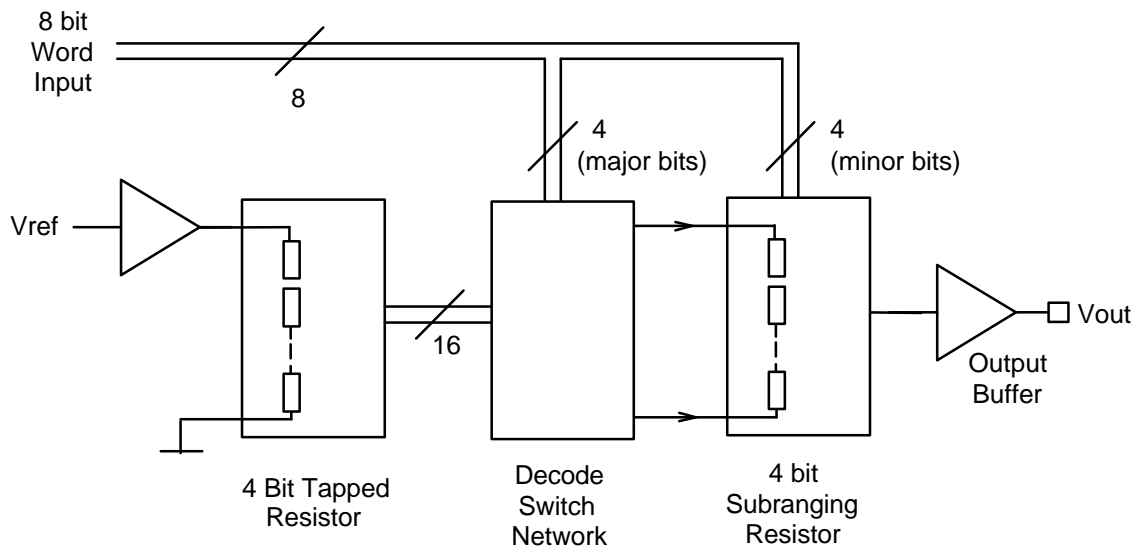
The tapped resistor is connected between an internal reference and ground in order to ease the input common mode range requirements of the output buffer.

The choice of the output buffer is dependant on the load and speed requirements: e.g. 2 μ s settling into 200pF with 5V output range.

Features

- CORE settling time typically 1 μ s
- $\pm 1/2$ lsb differential non-linearity
- Full scale output adjustable by varying gain of buffer
- Core quiescent current nominally 400 μ A

Functional Block Diagram



General Purpose ADC

Description

This minor ACSC function is a CMOS 8-bit linear successive-approximation charge-redistributed ADC with auto-zero and internal sample and hold.

During the first half of the conversion period, the input signal is buffered and sampled onto a hold capacitor whilst the comparator is auto zeroed.

The conversion itself proceeds on a successive approximation basis by sequentially switching

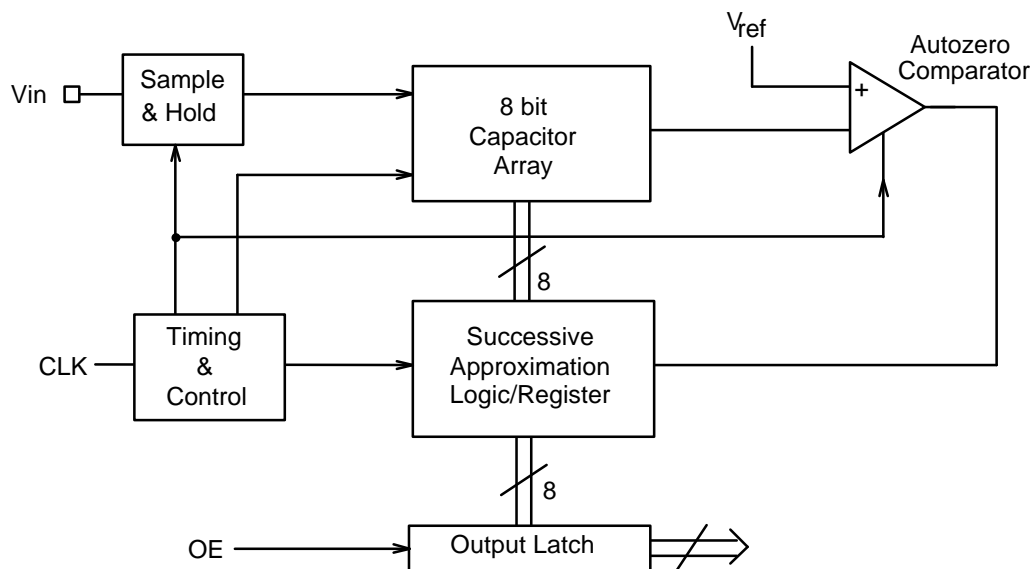
progressively smaller capacitors until the output of the capacitor array equals the reference V_{ref} . The switching is controlled by the successive approximation logic which makes a decision for each bit based on the comparator output.

The required 8 bit binary result appears at the output of the SAR block at the end of conversion and may be latched.

Features

- Typically 3 μ s conversion time
- $\pm 1/2$ lsb differential non-linearity
- 0V to V_{DD} analog input range with sample and hold
- Inputs may be multiplexed
- Slew rate, tracking is typically 2.5V/ μ s
- Quiescent supply current nominally 500 μ A

Functional Block Diagram



High Resolution ADC

Description

A basic cyclic converter can achieve a limited resolution due to the inaccuracy of the times 2 multiplier, the sample/hold feedthrough, and the amplifier gain used in its construction. This minor ACSC function is a high-resolution converter which removes these inaccuracies while still using the sequential conversion technique of any cyclic converter. Thus the rate of conversion is determined by the required resolution and the settling time but, now, conversion can be made to exceed 12 bits with 1 LSB integral non-linearity.

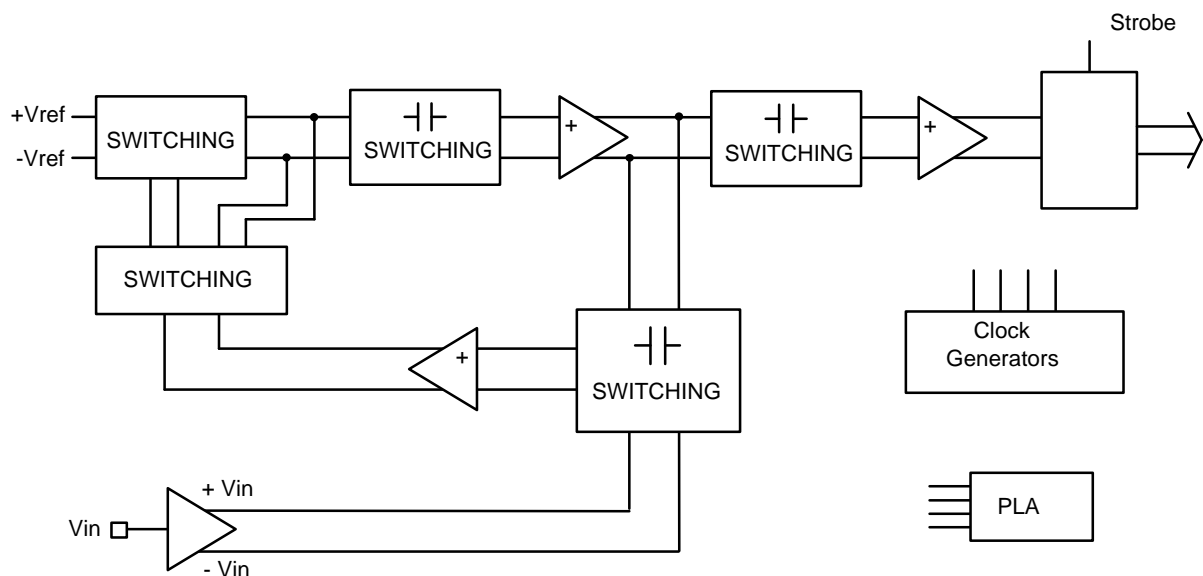
The reference voltage (initially set equal to the MSB) is rotated around the converter loop, interleaved with the

normal cyclic conversion algorithm. This causes the reference voltage to be subjected to the same converter loop tolerances (identified above) as the processed signal. This also relaxes the tolerance and size of the capacitors. Each bit of conversion must take 8 clock cycles in this converter and so the 12 bits requires 96 clock cycles in total. The structure used on this chip employs differential circuitry throughout and the capacitors are switched around the opamps to provide the functions of comparison, subtraction and multiply by 2. The switching and sequencing is provided by an on-chip PLA.

Features

- 12 bits resolution
- Single-chip solution with no external components except crystal oscillator
- Conversion rate of greater than 10kHz
- $\pm 5V$ supply
- No 'calibrate cycle' required
- Built in sample/hold
- Low power consumption (15mW)

Functional Block Diagram



Multiplying DACs

Description

Multiplying DACs are used to provide digitally controlled gain or attenuation.

The basic configuration shown in Fig. 1 uses an R-2R DAC in current steering mode and a trans-resistance stage with feedback resistor equal to R to provide a digitally controlled attenuator with a bandwidth determined by the amplifier. The addition of an amplifier, as in Fig. 2 gives bipolar operation.

For switched capacitor circuits, the R-2R DAC is replaced by a binary weighted capacitor array as shown in Fig. 3. The circuit provides bi-polar gain /

attenuation, where the inversion is achieved by changing the input switch phases.

In applications requiring logarithmic gain/attenuation increments the circuit of Fig. 4 can be used to provide an approximately logarithmic variation between gains A1 and A2 if:

$$\frac{C1}{C2} = \sqrt{A1 \times A2}, \frac{C1A}{C2} = A1 - \sqrt{A1 \times A2}$$

$$\frac{C2A}{C2} = \sqrt{\frac{A2}{A1}} - 1$$

Features

- Digitally controlled gain or attenuation
- Unipolar and bipolar configurations
- Continuous time and switched capacitor circuits
- Approximately logarithmic gain step circuit

Functional Block Diagram

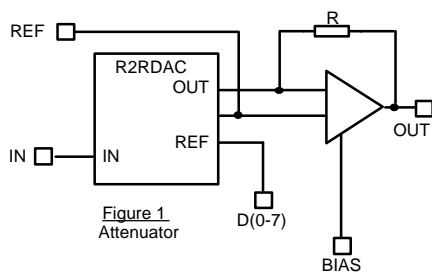


Figure 1
Attenuator

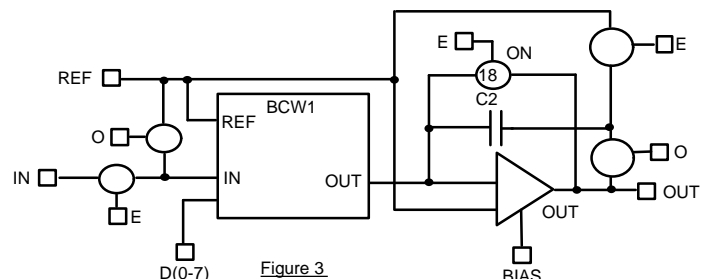


Figure 3
Switched capacitor
Bipolar gain

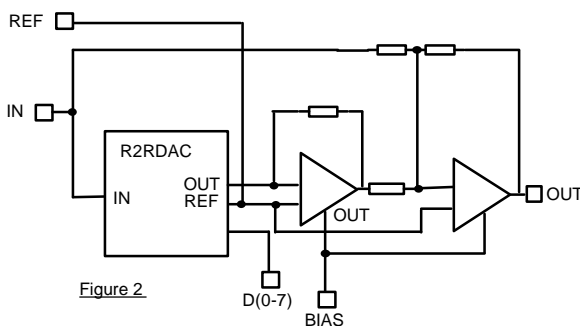
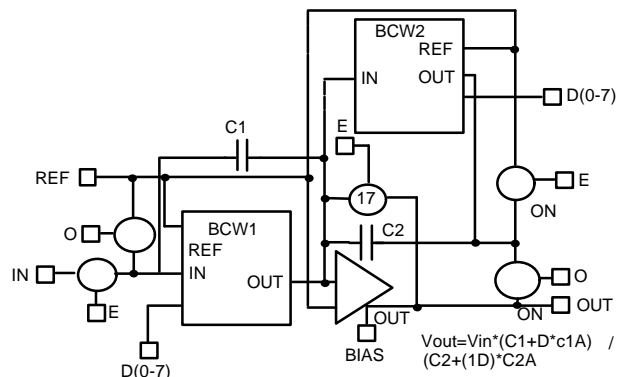


Figure 2



$$V_{out} = V_{in} \cdot \frac{C1 + D \cdot c1A}{C2 + (1D) \cdot C2A}$$

Figure 4
Switched capacitor
pseudo log gain

Band-Gap Reference

Description

This minor ACSC function is a CMOS Band-gap reference cell for use as an on-chip voltage reference.

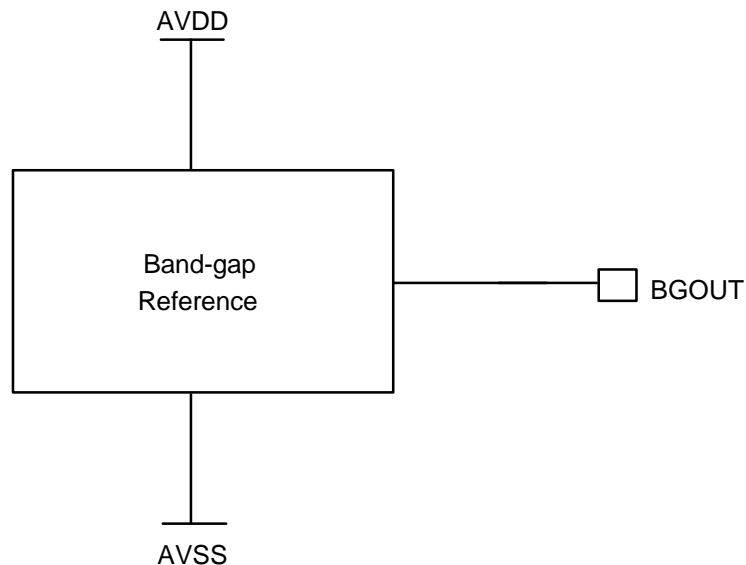
The cell uses vertical pnp transistors in the band-gap cell to reduce output voltage spread. A low offset and low noise bipolar amplifier is used to provide the loop gain.

The cell has an output impedance of 5k ohm so the output should be buffered for load currents exceeding 10 μ A.

Features

- 1.24 Volt reference \pm 4%
- Supply voltage range 2.5V to 6V
- Temperature coefficient < 100 ppm/ $^{\circ}$ C
- Power supply rejection ratio of >60dB
- Undecoupled output noise < 500 μ V r.m.s.

Functional Block Diagram



Hard Limiter

Description

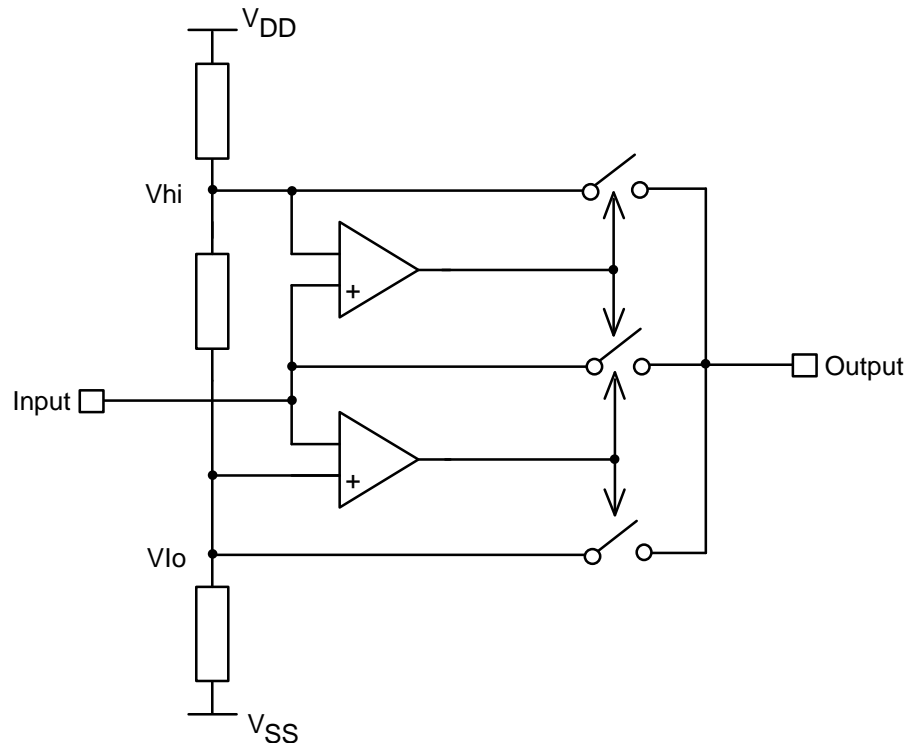
This minor ACSC function is a limiter consisting of two comparators and three switches that clamp the output to the high and low limiting voltages. This type of circuit operates with signals from DC to audio frequencies. The speed of the comparator will determine the upper frequency response of the limiter.

The reference voltages can either be generated as a ratio of the supply voltages, as shown, or derived from a known reference, for example a bandgap.

Features

- Operates from DC to audio frequencies
- Limiting levels set by resistor ratio

Functional Block Diagram



Soft Limiter

Description

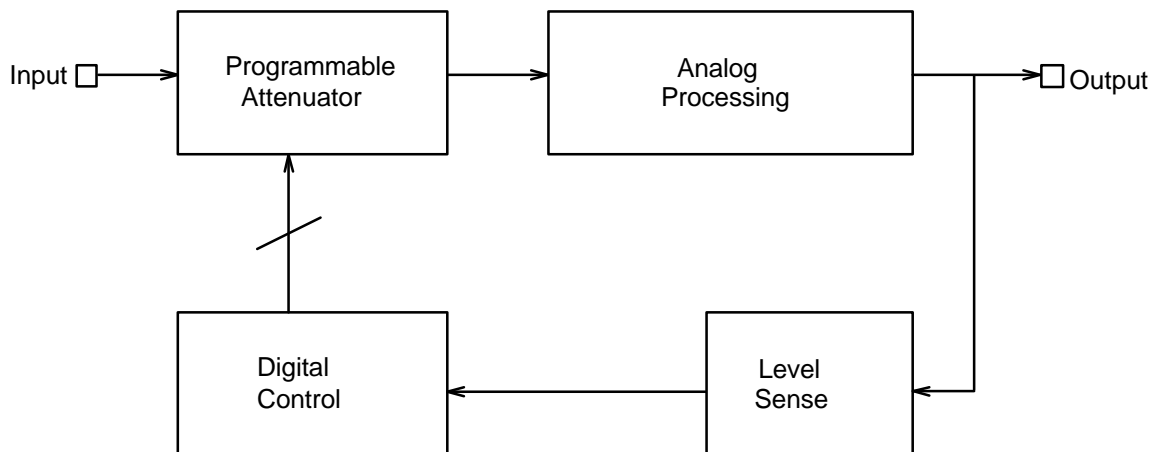
This minor ACSC function is a soft limiter consisting of a gain stage, level sense and digital controller in a closed loop. The signal amplitude is controlled using a digitally programmable attenuation stage driven from an up/down counter. The attack and decay rates are set

in the up/down count speed. The level sensing occurs after any system signal processing (for example filtering) and causes the digital control to count up when the preset limit is exceeded.

Features

- Attack / decay time set in digital controller
- Level sensing requires only a simple comparator
- Preset limit for the sense can easily be made ratiometric with supply voltage

Functional Block Diagram



Full Wave Rectifier

Description

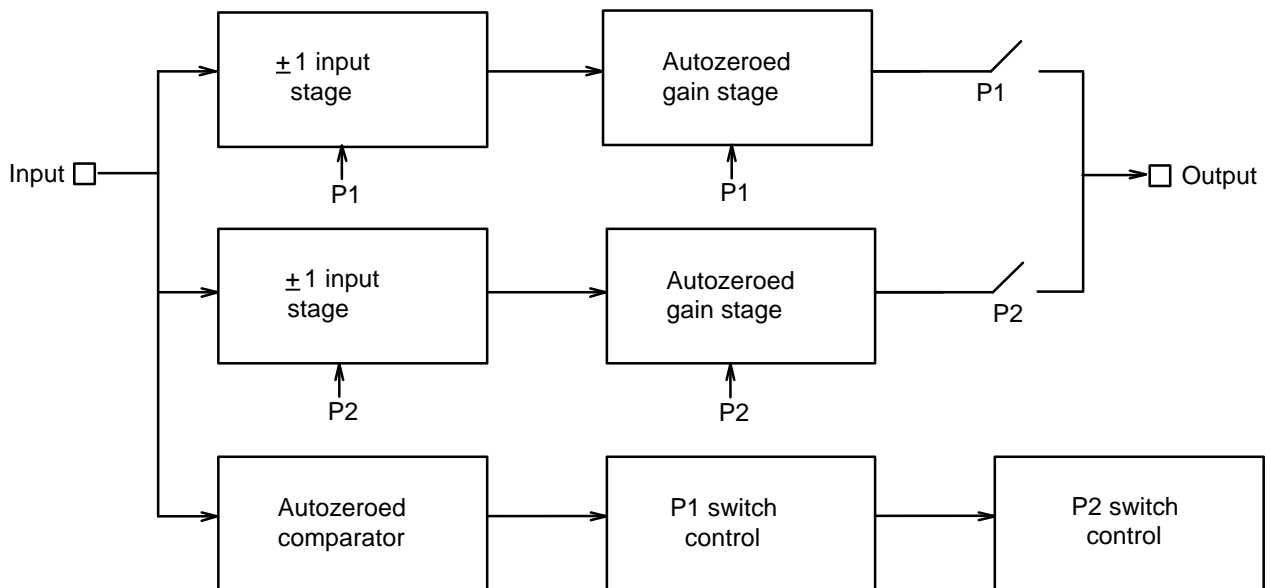
This minor ACSC function is a full wave rectifier, built using two interleaved rectifiers to generate a continuous output. Each rectifier consists of a ± 1 gain stage followed by an autozeroed switched capacitor gain stage. This cancels any amplifier input offset, and gives an accurate gain (due to the matching of the capacitor ratio).

The polarity of the input is sensed using an autozeroed comparator that drives the P1 and P2 switch control circuits.

Features

- Low input offset circuit
- Continuous output
- Accurate gain due to SC structure

Functional Block Diagram



Battery Voltage Detector

Description

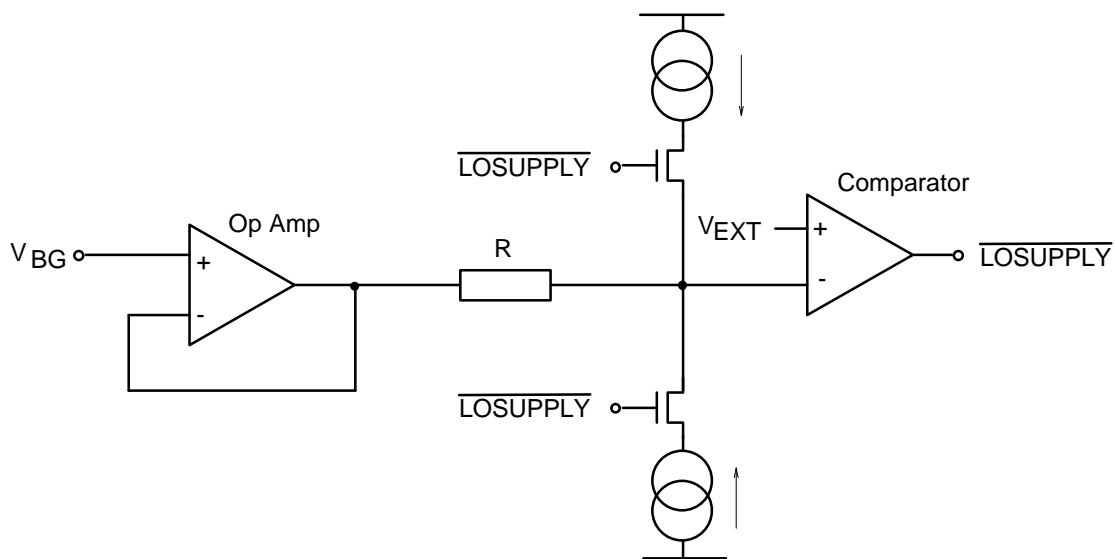
This minor ACSC function is a battery voltage monitor where a buffered bandgap reference voltage is compared to an external voltage, and output LOSUPPLY goes low when $V_{EXT} < V_{TRIP}$. The use of the bandgap reference voltage allows an accurate and temperature stable threshold to be defined.

The positive trip level, as V_{EXT} falls towards V_{BG} , is $V_{BG} - IR$. When $V_{EXT} < V_{BG} - IR$, LOSUPPLY goes low, moving V_{TRIP} to $V_{BG} + IR$. Appropriate choice of I and R allows any noise on V_{EXT} to be rejected, and not cause false triggering of LOSUPPLY.

Features

- Comparator and bandgap reference voltage allows accurate voltage detection
- Incorporates hysteresis to prevent false triggering and output glitches
- Use of external potentiometer allows voltages outside of the supply range of the device to be monitored
- Useful in low battery voltage detection circuits

Functional Block Diagram



Voltage Regulator

Description

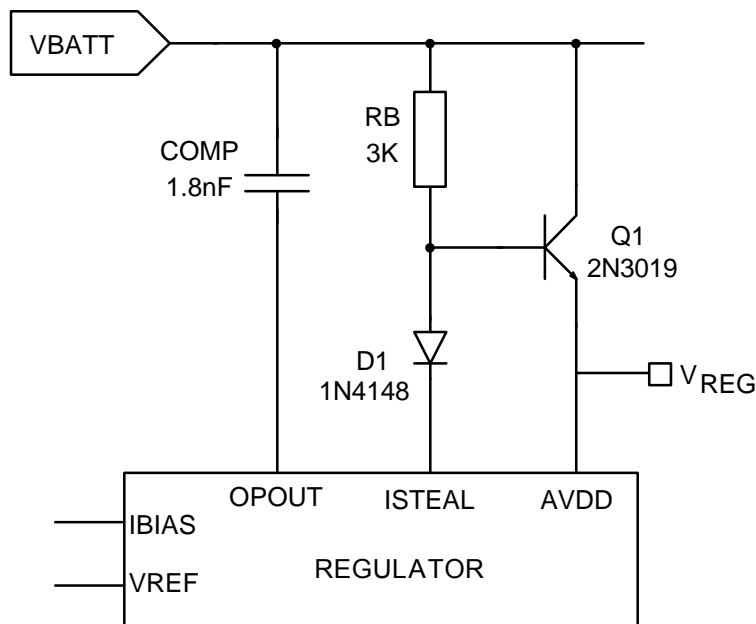
This minor ACSC function is a 5V voltage regulator and requires just 1 resistor, 1 diode, 1 npn transistor and 1 capacitor to function. It is capable of providing up to 12mA at 5V. The output is accurate to 10% over

the temperature range 0-70°C and for input voltages between 6V and 16V.

Features

- 6-16V input voltage range
- 5V \pm 10% output voltage
- 12mA current capability
- Uses just 4 external components

Functional Block Diagram



Diagnostic Universal Asynchronous Receiver Transmitter

Description

This major ACSC allows, with a minimum external connections, the transfer of large amounts of data to and from mixed signal ASICs.

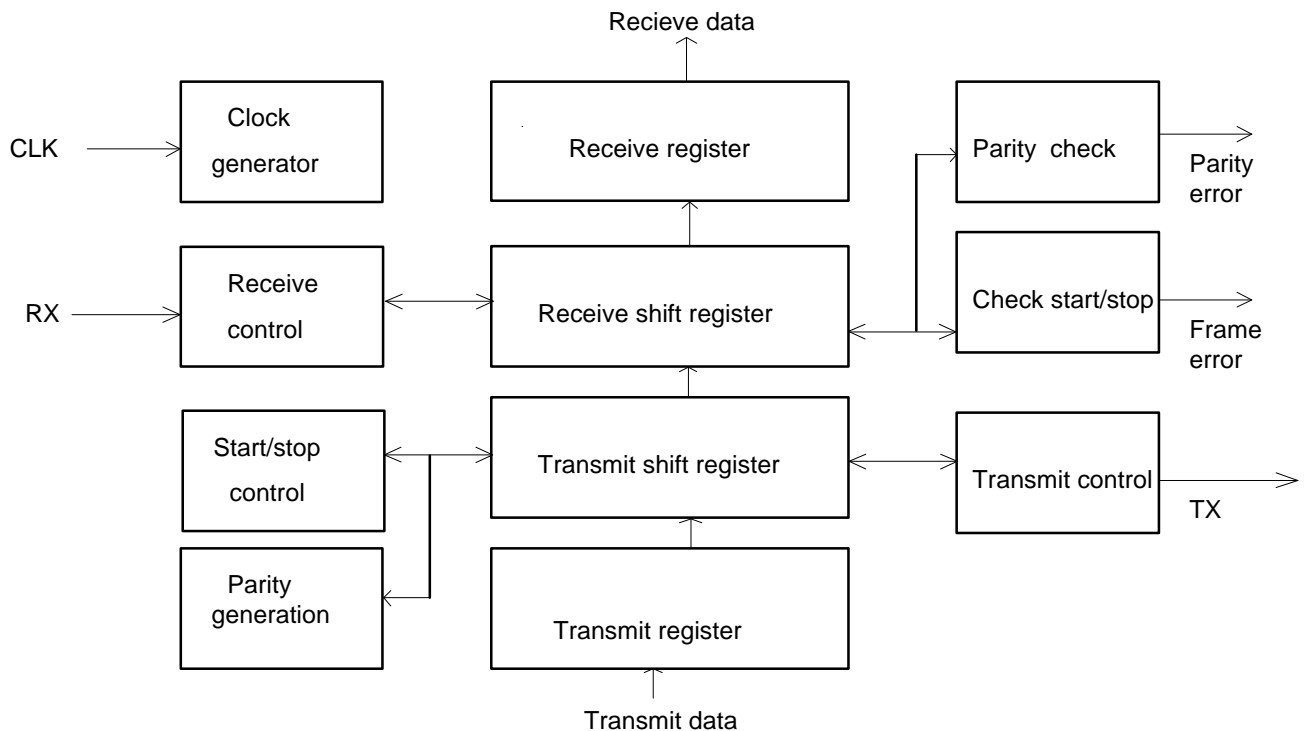
The UART function is an industry standard serial interface and is implemented in many micro-controller

devices. It allows 8 bit data to be asynchronously transferred bi-directionally between 2 systems. The data is transparently processed by the UART which means there is no protocol overhead in such a system.

Features

- Compatible with industry standard UARTs
- Duplex operation
- Start, stop and parity generation and recognition
- Cost effective solution for connecting mixed signal ASICs to computer diagnostic aids
- -40°C to +120°C operation
- Single +5V supply

Functional Block Diagram



Hall Effect Switch

Description

The Hall Effect switch is based on two MOS devices with split drains. With a magnetic field perpendicular to the silicon, the path of the majority carriers in the MOS channels are deflected. When the two devices drains cross coupled, the paths for the positive charged 'holes' and negative charged 'electrons' are deflected in opposite directions which causes a differential output.

A comparator then detects the differential output to give a north or south pole indication.

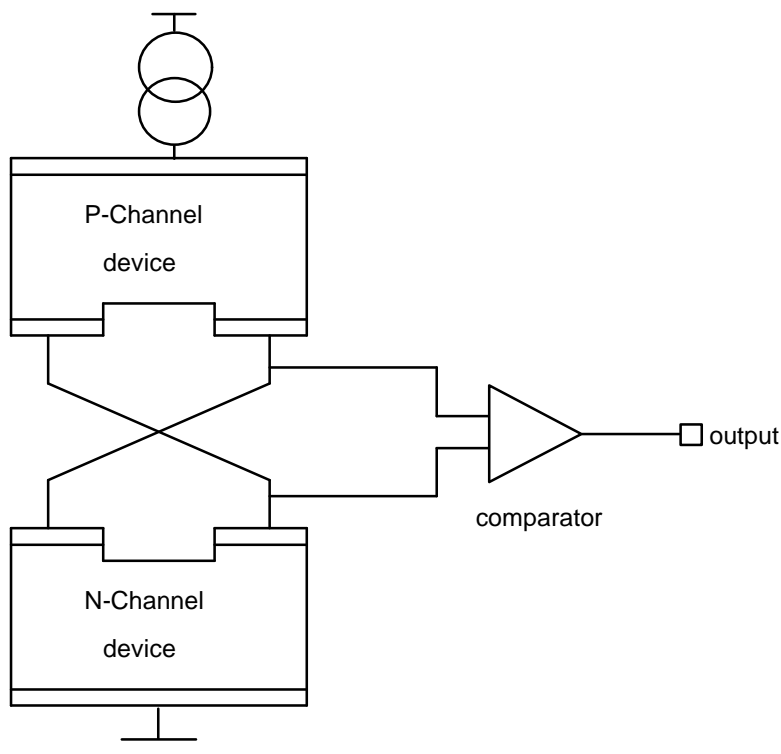
Applications for this device include position sensing, revolution counters, etc.

Due to the small size the circuit is easily embedded within additional circuitry to give an intelligent sensor.

Features

- Small area
- North/South pole output
- Temperature and process compensated design

Functional Block Diagram



DTMF GENERATOR

Description

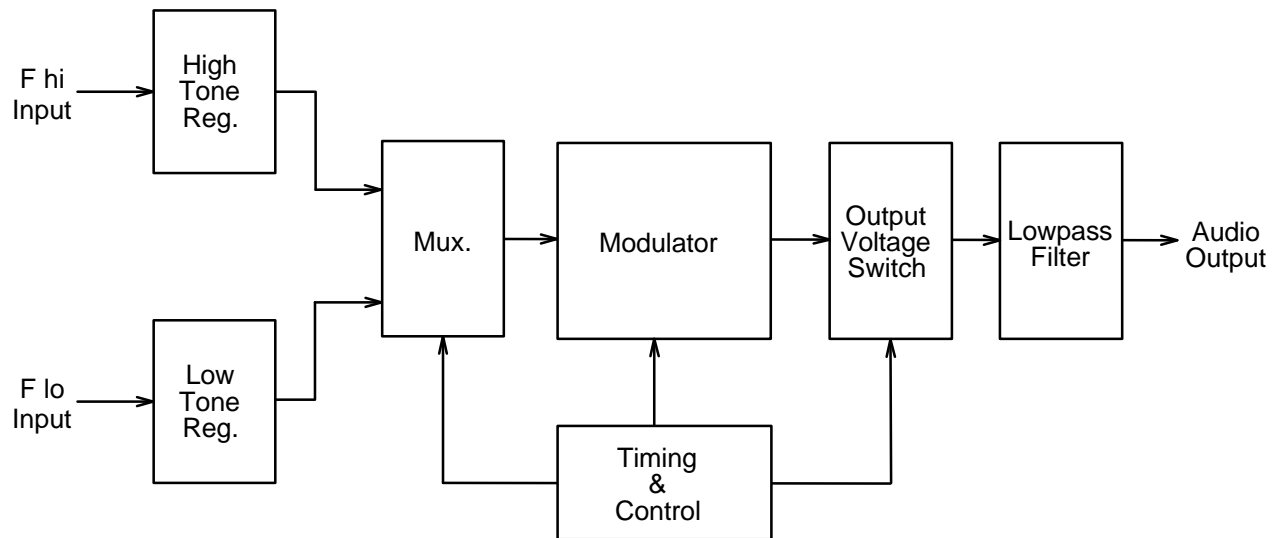
This major ACSC function employs an oversampling frequency synthesiser in an interleaved mode to produce dual-tone multi-frequency (DTMF) telephone dialling tones. The synthesiser is based on direct digital synthesis using phase accumulation with the high and low tone frequency divisors held in separate input registers. The digital to analog conversion is carried out

using a first order sigma-delta converter which interleaves the high and low tone samples. The 1-bit datastream switches two bi-polar voltage levels to produce the fixed tone twist for the CCITT specification. The output is then filtered using a simple 2nd order lowpass filter to regenerate the audio signal.

Features

- Low power requirements - logic based
- Small size
- Perfected for mobile communications applications

Functional Block Diagram



SERIAL INTERFACE ADAPTOR (LANCE)

Description

This major ACSC function is an IEEE 802.3/Ethernet compatible Manchester Encoder / Decoder, that integrates all functions to interface Local Area Network Controller for Ethernet (LANCE) to the Ethernet transceiver cable. It has two sections, transmitter and receiver. The transmitter uses Manchester encoding to clock data into a serial bit stream, differentially driving up to 50m of twisted pair

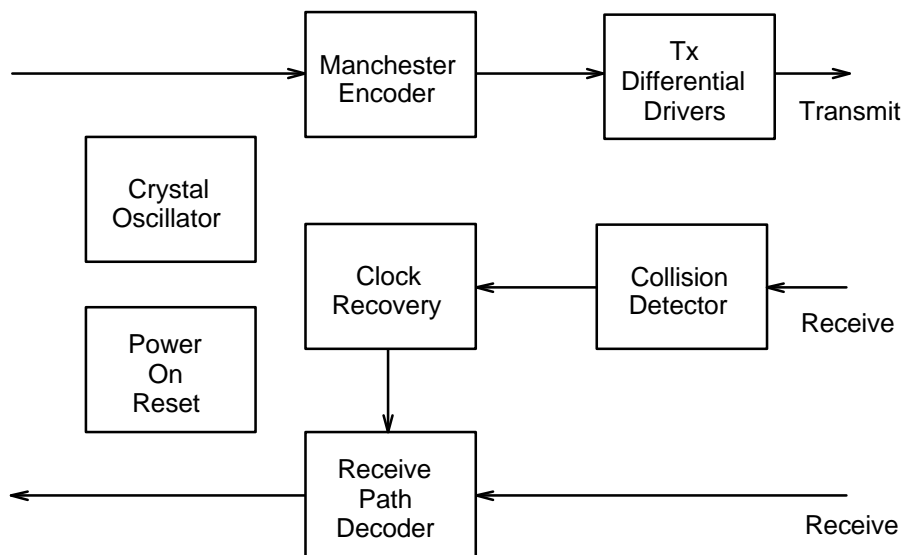
transmission line. The receiver detects the presence of data and collisions. The receive clock is recovered from the incoming bit stream by a phase locked loop and is used to decode the Manchester bit stream into data.

The cell can be programmed to operate in one of two variants compatible with the SIA types 8023 and 7992.

Features

- Compatible with Ethernet/IEEE-802.3 specifications
- 20 MHz parallel resonant crystal oscillator
- Manchester Code Encoder and Decoder
- Phase Locked Loop Clock Recovery
- Loopback Diagnostic Test Capability
- Receiver and Collision Squelch Circuit guarantees operation at inputs $\geq \pm 275\text{mV}$ and with no operation $\leq \pm 160\text{mV}$
- Emulates most common SIA alternatives

Functional Block Diagram



CODEC

Description

This major ACSC function implements a 13 bit 8kHz PCM speech encoder/decoder and the associated speech channel filtering using a sigma delta modulator and DSP techniques.

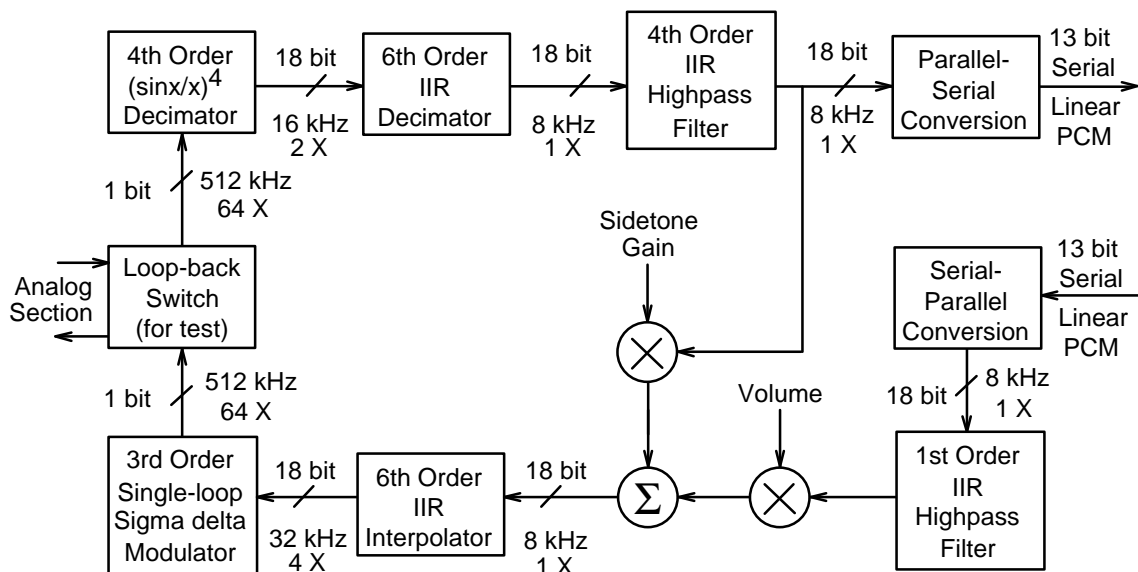
The sigma delta modulator oversamples at 512kHz, which is decimated to 16ksp in a $(\sin x/x)^4$ filter. The encoding channel filter is a 10th order band pass filter.

The input data is scaled by the volume control and the sidetone (also programmable level) is added. The decoding channel filter is a 6th order lowpass at 32ksp which is followed by a digital sigma delta modulator to generate the 512kHz bit stream which is converted to analog, filtered and output.

Features

- 13 bit 8kHz PCM speech codec and filters
- Sigma delta modulator / DSP implementation
- Meets CCITT filter requirements
- Programmable receive volume
- Programmable Sidetone
- Scalable to lower operating voltages
- Used in telephone / mobile handsets

Functional Block Diagram



SPEECH COMPANDER

Description

This major ACSC function processes telephone bandwidth (300Hz to 3.4kHz) audio signals according to a 2:1dB logarithmic law. The compression and expansion processes use the same basic cells in a different configuration.

The compressor uses a delta-sigma converter with variable reference voltage generated by full wave rectifying and filtering the audio output. The bit stream data is then multiplied by a fixed reference voltage and the audio output generated by the reconstruction filter.

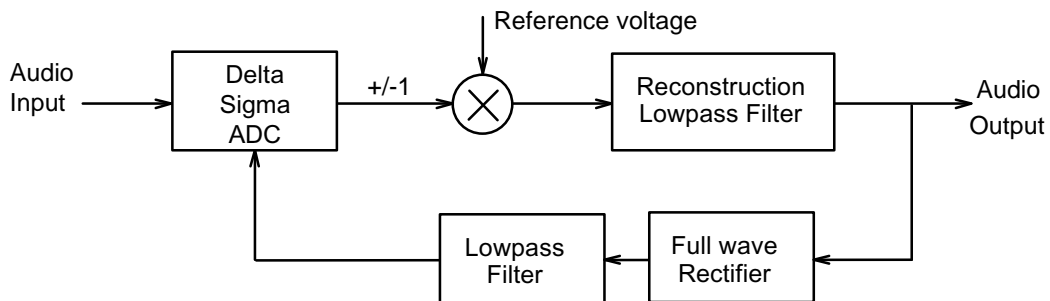
The expander uses a delta-sigma converter with a fixed reference voltage. The input is also full wave rectified and lowpass filtered to give a variable reference. The bit stream data is then multiplied by the variable reference and the audio output generated by the reconstruction filter.

Features

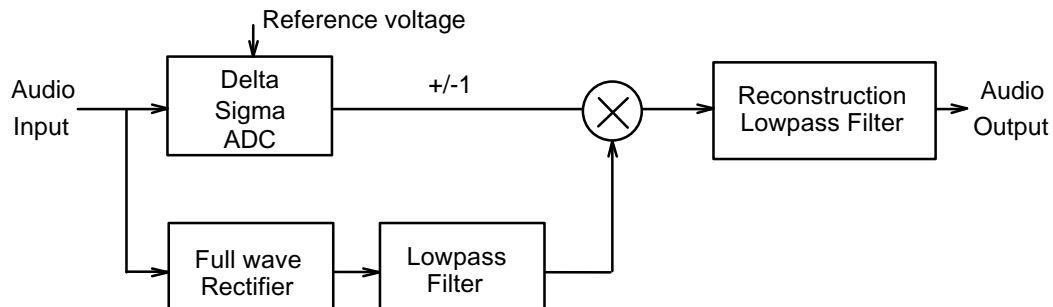
- Small size
- Implemented on CMOS technology
- Low external component count

Functional Block Diagram

COMPRESSOR



EXPANDER



OVER-VOICE MODEM

Description

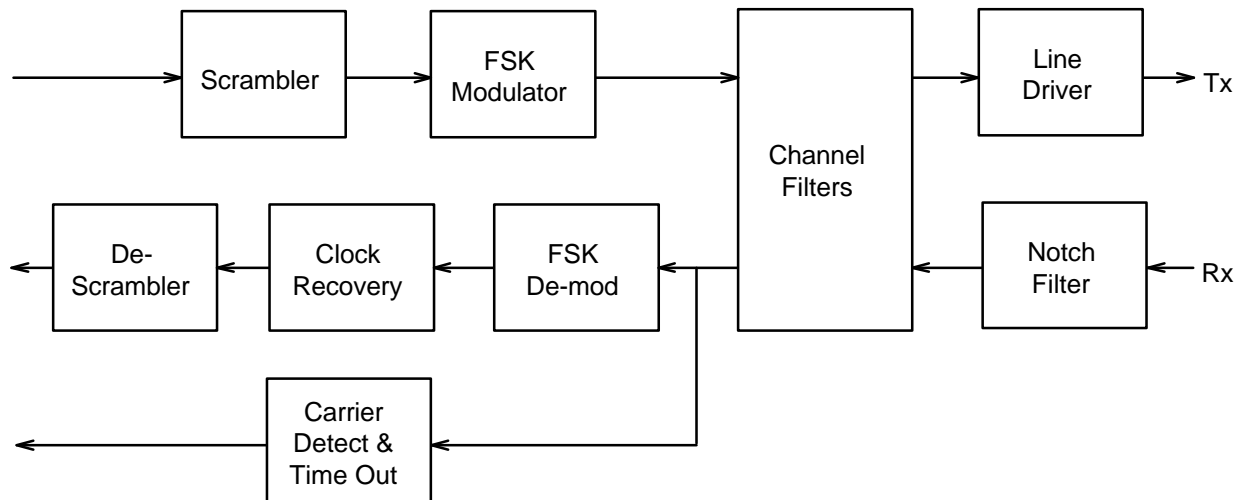
This major ACSC provides all the functions required for an 'over-voice' modem, which transmits and receives data at 4800 baud over the standard telephone line such that the data channel does not interfere with normal voice communication. The transmit portion of the circuit employs phase coherent FSK modulation using a synthesised sine wave to produce a Space tone at 17.55KHz and a Mark tone at 21.94KHz. The modulated signal is band-pass filtered and buffered before application to the line. Operation is in half-duplex mode and synchronous or asynchronous transmission can be selected. In synchronous mode the data is scrambled.

The receive function includes switched capacitor filters for filtering the FSK signal and rejecting the 12KHz Pay-tone, a zero-crossing detector and digital demodulator, the demodulated signal is reconstructed via a switched capacitor low-pass filter and a comparator. There is also a carrier detect circuit which detects that the carrier is of correct frequency and amplitude for operation of the receiver.

Features

- Phase coherent FSK modulation
- Transmission rate 4800 baud
- Half-duplex synchronous / asynchronous operation
- Carrier detection
- No external filter components
- +5V single supply
- Low consumption 4mA typical
- Loop-back mode for testing overall functionality

Functional Block Diagram



SPEECH SCRAMBLER/DESCRAMBLER

Description

This major ACSC function performs scrambling and descrambling operations on speech (300Hz to 3.4KHz) signals. The input speech signal is filtered into four bands which are then modulated onto one of the other bands with or without frequency inversion, thus resulting in approximately 100 usable scrambling codes. The de-scrambler is used to restore the original speech after transmission.

The input is first filtered by on-chip CT anti-alias filters prior to anti-alias filtering by a switched capacitor filter for the sampling rate used in the signal path also by use of switched capacitor circuitry. The input filter bank consists of four filters which split the speech into four bands of 800Hz.

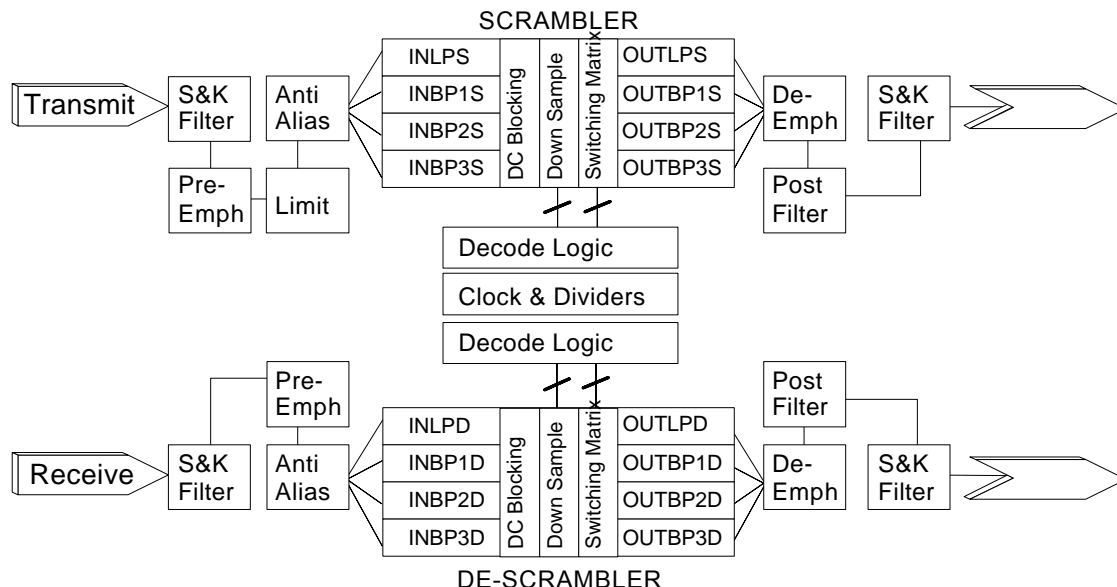
To avoid tones at the carrier frequencies caused by DC modulation, DC offset cancellation is included in each path. A matrix of switches is provided to enable any input channel to be routed to any output channel and is controlled by an 8-bit word. Each input frequency band is down-sampled by taking every eighth sample and discounting the intervening samples. By multiplying alternate samples by -1 a frequency shift of 800Hz is obtained and it possible to map an input band onto any output band. Output filters are adjusted to give the required $\sin(x)/x$ correction due to the sampling rate.

The four output bands are summed prior to the de-emphasis filter and, on the transmit side, this results in a scrambled speech signal - on the receive side de-scrambled speech is obtained.

Features

- Functions from single 5V supply
- Less than 6mA power consumption
- Contains both scrambler and de-scrambler on one chip
- Contains all filters on this single chip
- Very few external components
- Controlled via serial interface
- For commercial specification security systems
- For use in both base-stations and mobile handsets

Functional Block Diagram



SWITCHED CAPACITOR FILTERS

Description

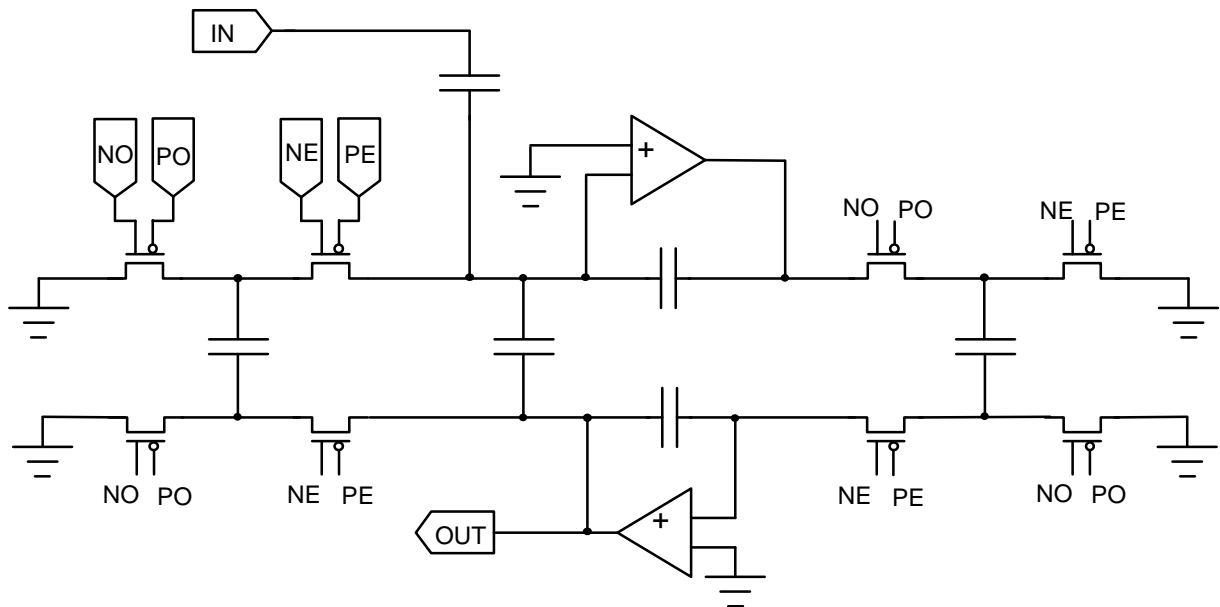
By using state-of-the-art CAD tools for design, synthesis and simulation of sample-data filters either cascaded biquad or RLC ladder filters may be provided using switched-capacitor realisations with orders from 1 to > 12. For flexible, programmable and area-efficient filter structures, any number of 1st, 2nd and 3rd-order biquad sections may be cascaded and then simulated for effects of supply voltage, process and temperature variations prior to synthesis.

Dynamic range and frequency response can be extended by use of fully differential structures. $\sin(x)/x$, warping and aliasing effects are reduced by pre-warping the filter response and by use of 2nd or 3rd order continuous-time (active RC) filters which are included on chip. Filter sensitivity is reduced by use of ladder, rather than cascaded biquad, SCF structures. Non-overlapping clock phases required by the SC switches are generated using standard cell circuits.

Features

- Handles signal frequencies from <0.1Hz to >250kHz
- Uses on-chip anti-aliasing filters
- No external (off-chip) components required
- Either $\pm 5v$, +5v or +3v supplies may be catered for
- Clock phases generated on-chip from just one external (stable) clock
- Gains and pole positions accurate to within 0.05%
- Filters, integrators, differentiators, rectifiers and companders may be realised

Functional Block Diagram (2nd Order Biquad)



DIGITAL FILTERS

Description

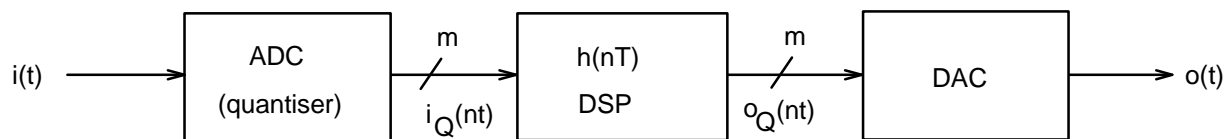
When reproducible, accurate and/or programmable filtering is required in a single-chip solution a digital filter should be considered. Using state-of-the-art design tools and technologies, DSP solutions can be provided to a wide range of datacom, telecom, audio, medical and consumer requirements. These may be used in conjunction with mixed-signal cells such as amplifiers, CT-filters, ADCs and DACs as exemplified in the schematic below. Using Mentor Graphics' DSP Station the filter is designed, optimised and simulated at gate/block level for a bit-true realisation.

Finite word-length analysis, limit-cycle investigations and noise analyses are carried out prior to transfer for ASIC routing tools for area-efficient synthesis. VHDL may also be used for design entry, simulation or logic synthesis. Code is generated for use in prototyping (FPGA or DSP board) when hardware is required prior to silicon availability.

Features

- Filters of virtually any order may be realised
- Supply voltages of 2.7-5v catered for
- Supported by prototyping
- Operation may be programmable
- FIR or IIR
- Adaptive filters
- May be used in conjunction with on-chip data-converters for analog-in/analog-out integration

Functional Block Diagram



OSCILLATOR FOR CERAMIC RESONATORS

Description

This minor ACSC is a 2-pin oscillator based on a single-stage class A amplifier. This minimises the output voltage swing and therefore current/power dissipation.

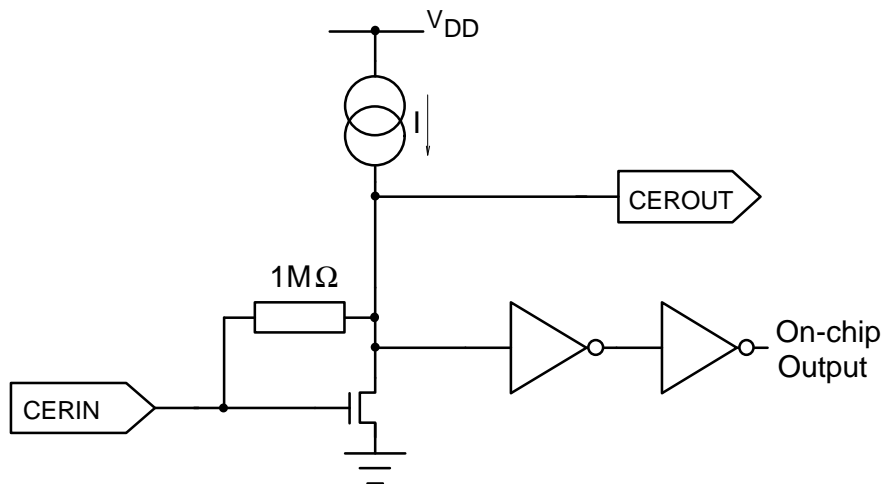
An internal $1M\Omega$ (nom.) feedback resistor is provided, saving an external component. The oscillator cell, when used with a resonator with integral load capacitors provides a low-cost and compact stable timebase for many applications.

At 4MHz, $I_{DD} < 200\mu A$ (nom.)

Features

- 2 pin oscillator, well suited for use with ceramic resonators
- Frequency range 0.5MHz to 4MHz
- Feedback resistor ($1M\Omega$) on-chip saves external component
- Operating current $200\mu A$ or less

Functional Block Diagram



CRYSTAL OSCILLATOR

Description

This minor ACSC function is a 2-pin oscillator intended for use with crystals and ceramic resonators.

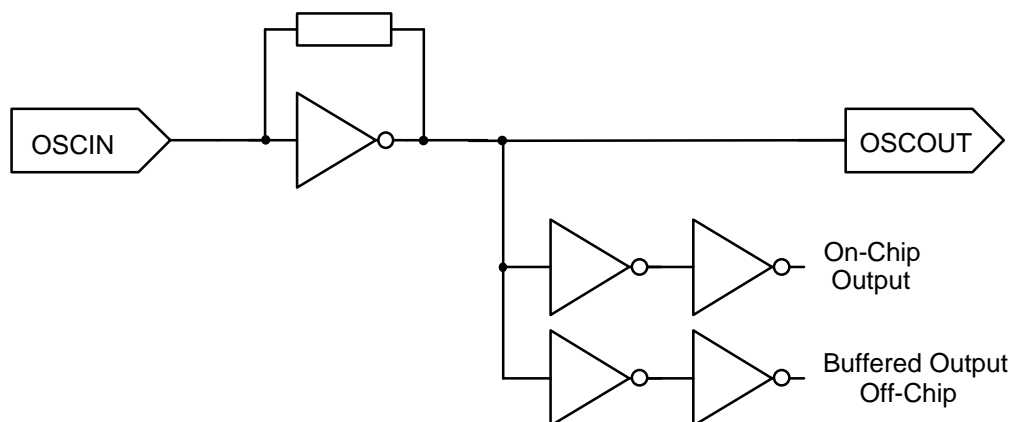
An internal $1\text{ M}\Omega$ (nom.) feedback resistor saves an external component and simplifies board layout.

The output of the oscillator can be buffered and brought off-chip through a suitably-sized driver to provide a system clock to the rest of the board.

Features

- 2 pin oscillator, suited to use with ceramic resonators from 6 to 12MHz, or crystals up to 20MHz
- Internal $1\text{ M}\Omega$ (nom.) feedback resistor saves external component
- Operating current with 12MHz resonator typically 1.5mA

Functional Block Diagram



RC OSCILLATOR

Description

This minor ACSC function is a 1-pin relaxation oscillator. Frequency variations for $f < 1\text{KHz}$ is primarily set by external components.

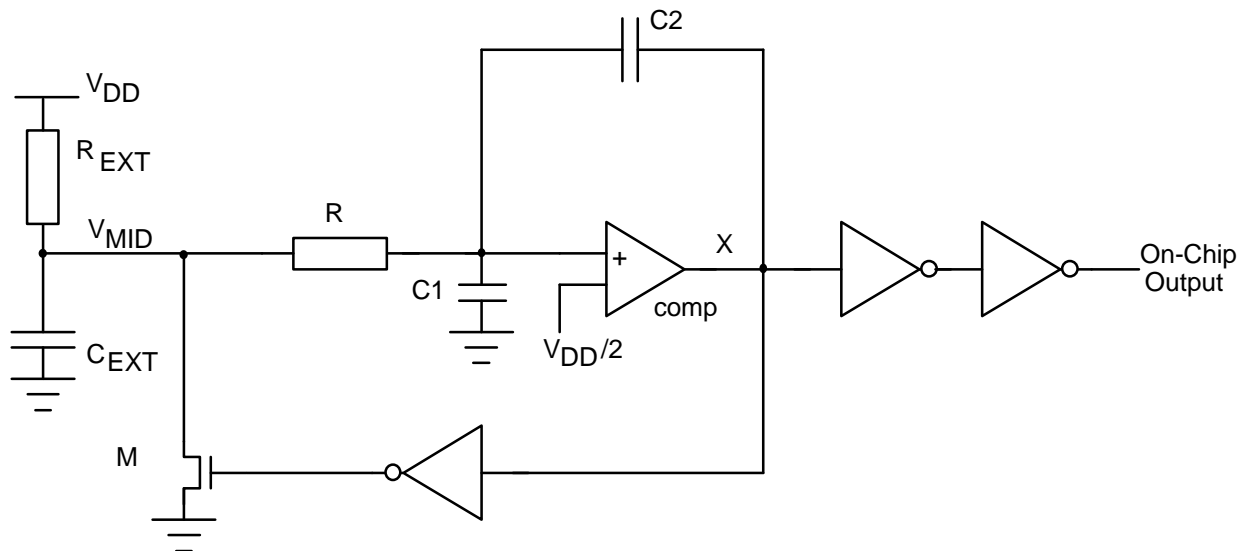
$$t_{\text{osc}} = 0.693 (R_{\text{EXT}} C_{\text{EXT}} + 6\mu\text{s})$$

As V_{MID} crosses $V_{\text{DD}}/2$, comp output x goes high, switching on the pull down device M, for time $RC1$, completely discharges V_{MID} to 0V. M then switches off, causing V_{MID} to charge up towards V_{DD} again.

Features

- Single-pin oscillator, suitable for generating low-frequency clocks ($<1\text{KHz}$)
- Frequency determined by external R and C
- Low operating current for $R = 1\text{M}\Omega$, $C = 4.7\text{nF}$, $f = 310\text{Hz}$, $I_{\text{DD}} = 35\mu\text{A}$

Functional Block Diagram



LOW IMPEDANCE AUDIO DRIVER

Description

This minor ACSC function is an audio frequency 3 stage buffer with $\pm 12\text{mA}$ output current capability designed specifically to drive low impedance loads such as dynamic transducers.

A double folded cascode input stage provides high front end gain for the intermediate common mode gain stage.

Complementary source followers provide gate drive to the output MOSFETs whilst minimising crossover

distortion normally associated with class B output stages.

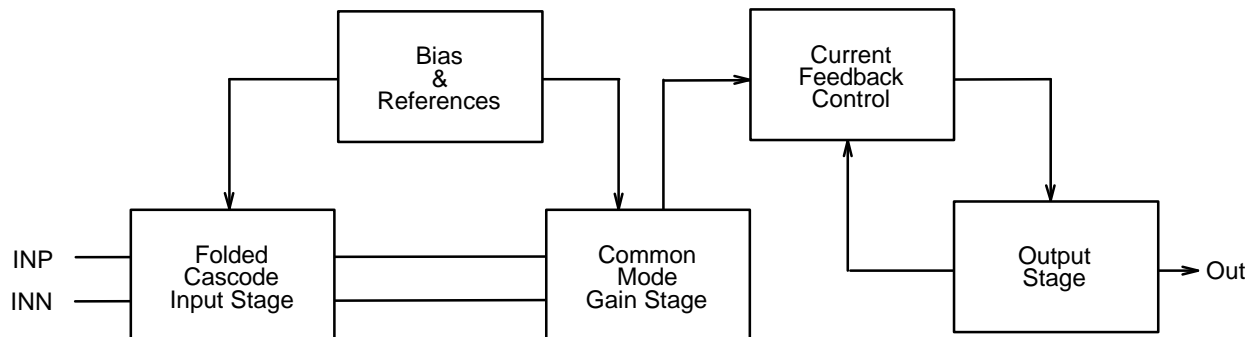
Supply current is minimised by use of a quiescent current feedback control block which monitors the output device current and adjusts the drive to the source followers whilst maintaining stability.

The buffer is internally compensated and will drive capacitive loads up to 100pF rail to rail.

Features

- High current drive buffer provides 4Vpp output into 180Ω with <0.5% THD ($V_{dd} \geq 4.8\text{V}$)
- Three stage design with current feedback control only takes 300μA typical quiescent current
- 105dB open loop gain 200KHz unity gain bandwidth 90dB PSRR at 1KHz
- Pair of drivers may be used to drive load differentially

Functional Block Diagram



LOW NOISE AUDIO AMPLIFIER

Description

This minor ACSC function is a MOSFET input low noise amplifier with rail to rail output buffer, designed for audio applications requiring a high input impedance.

The front end consists of P-channel cascoded input devices which have been sized with their loads to provide low flicker noise ($1/f$ knee $<100\text{Hz}$).

Noise performance is suitable for telephone applications; equivalent input referred noise from $50\text{Hz} - 3.4\text{kHz}$ is $1.6\mu\text{Vrms}$. Supply rejection exceeds 80dB across this band.

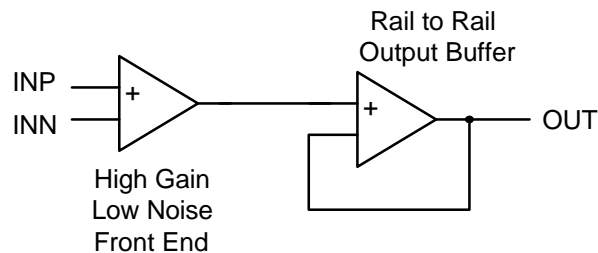
Thermal noise is $<25\text{nV/Hz}^{1/2}$.

The output buffer provides low distortion ($<0.05\%$ THD) for $\pm 2.0\text{V}$ in to $10\text{k}\Omega/50\text{pF}$.

Features

- High input impedance, low noise audio amplifier
- Configured with gain for optimum low noise audio path
- Cascoded front end provides $>80\text{dB}$ PSRR up to 4kHz
- Equivalent flat input referred noise typically $27\text{nV/Hz}^{1/2}$ over telephone bandwidth
- Supply current = $320\mu\text{A}$, $V_{\text{dd}(\text{min})} = 4.8\text{V}$
- Open loop gain = 120dB , Unity Gain BW = 1MHz

Functional Block Diagram



RAIL TO RAIL AMPLIFIER

Description

This minor ACSC function is an internally compensated, unity gain stable buffer.

True rail to rail operation is achieved by twin input stages with a low-gm, low distortion input crossover stage.

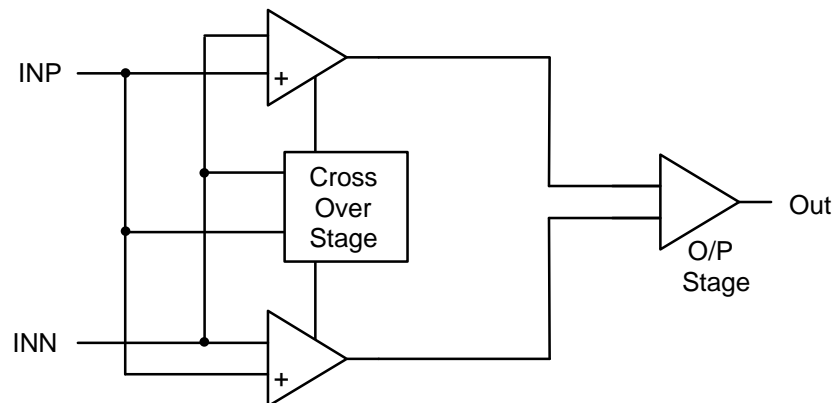
The pseudo push-pull output stage provides low distortion with low (250 μ A) quiescent current.

Open loop gain and bandwidth are 96 dB, 1MHz respectively.

Features

- Dual input stage gives rail to rail input common mode range
- Rail to rail output for capacitive loads up to 50pF
- $\pm 1.9V$ into 10K Ω load; $\pm 0.7V$ into 2.5K Ω load (Vdd=4.8V, THD \leq 30m%)
- Low supply voltage (2.7V) capability with rail to rail operation
- Higher output drive variant available ($\pm 2.1V_{pk}$ into 1K Ω , Vdd=4.8V, 500 μ A quiescent)

Functional Block Diagram



MID-REFERENCE BUFFER

Description

This minor ACSC function is a unity gain analog ground buffer with complimentary source follower outputs, providing matched output current capability.

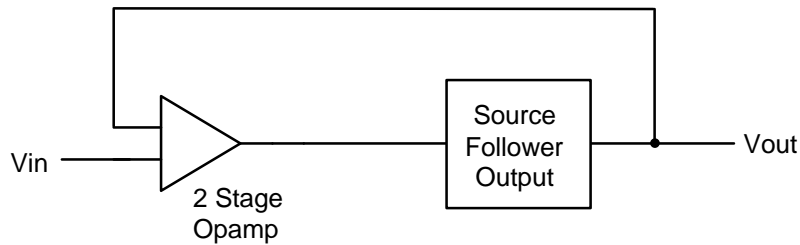
Internally compensated to remain stable for capacitive loads up to 100pF.

Nominal open loop gain and bandwidth is >75 dB and 600KHz respectively.

Features

- Less than 0.1% load regulation at 2.5V for 2.4mA output current
- Equal output current source and sink capability
- Low quiescent current 250 μ A
- High input resistance from MOSFET inputs

Functional Block Diagram



8 BIT GENERAL PURPOSE DAC

Description

This minor ACSC function is a medium speed CMOS 8 bit resistor sub ranging DAC with buffered voltage output.

Depending on the input code a 16 element sub ranging resistor (SubR) is connected across two adjacent taps of a 16 element tapped resistor. The four major bits determine the position of the SubR resistor on the tapped resistor whilst the minor bits decode the sub ranging resistor itself.

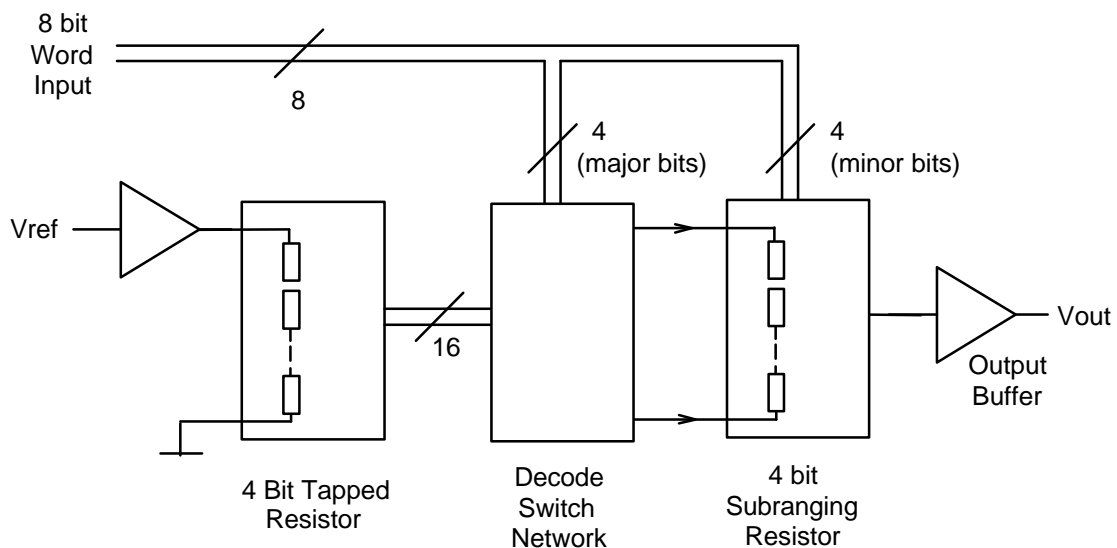
The tapped resistor is connected between an internal reference and ground in order to ease the input common mode range requirements of the output buffer.

The choice of the output buffer is dependant on the load and speed requirements: e.g. 2 μ s settling into 200pF with 5V output range.

Features

- CORE settling time = 1 μ s typical
- $\pm 1/2$ lsb differential non-linearity
- Full scale output adjustable by varying gain of buffer
- Core quiescent current 400 μ A typical

Functional Block Diagram



8 BIT GENERAL PURPOSE ADC

Description

This minor ACSC function is a CMOS 8-bit linear successive-approximation charge-redistributed ADC with auto-zero and internal sample and hold.

During the first half of the conversion period, the input signal is buffered and sampled onto a hold capacitor whilst the comparator is auto zeroed.

The conversion itself proceeds on a successive approximation basis by sequentially switching

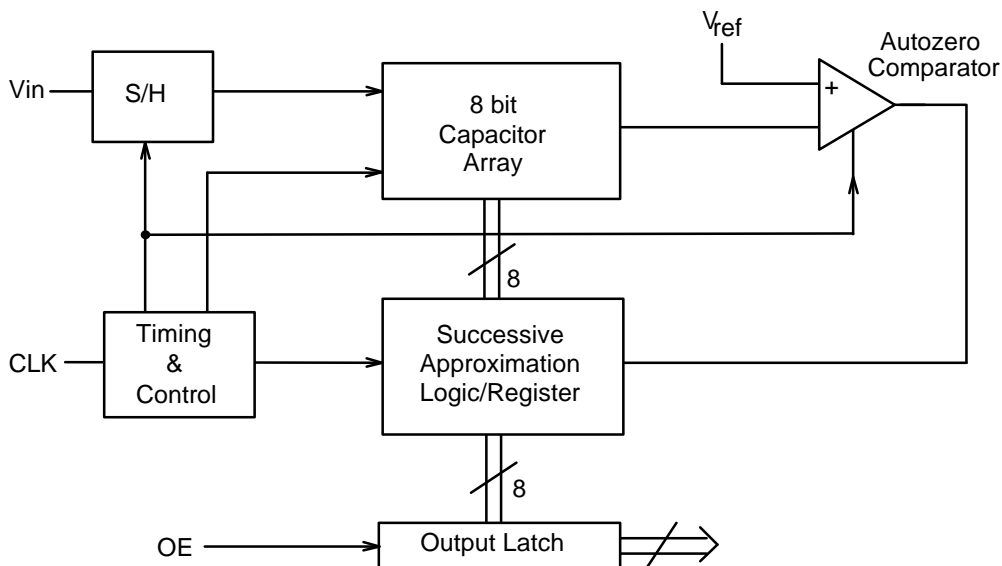
progressively smaller capacitors until the output of the capacitor array equals the reference V_{ref} . The switching is controlled by the successive approximation logic which makes a decision for each bit based on the comparator output.

The required 8 bit binary result appears at the output of the SAR block at the end of conversion and may be latched.

Features

- Typical 3 μ s conversion time
- $\pm 1/2$ lsb differential non-linearity
- 0V to VDD analog input range with sample and hold
- Inputs may be multiplexed
- Slew rate, tracking = 2.5V/ μ s
- Quiescent supply current 500 μ A typical

Functional Block Diagram



8 BIT VIDEO ADC

Description

This minor ACSC function is a high speed 8-bit ADC was designed for applications where fast conversions are needed (e.g. for digital video signal processing). To give the best compromise for high speed, low power dissipation and small silicon area, the most suitable structure is a half-flash ADC. The conversion is performed in 3 successive phases. In the first operation, the analog input voltage V_{in} is sampled. In the second phase, the most significant bits are determined and a DAC converts this coarse digital code to subtract it from the held input. In the last operation, the less significant bits are determined from

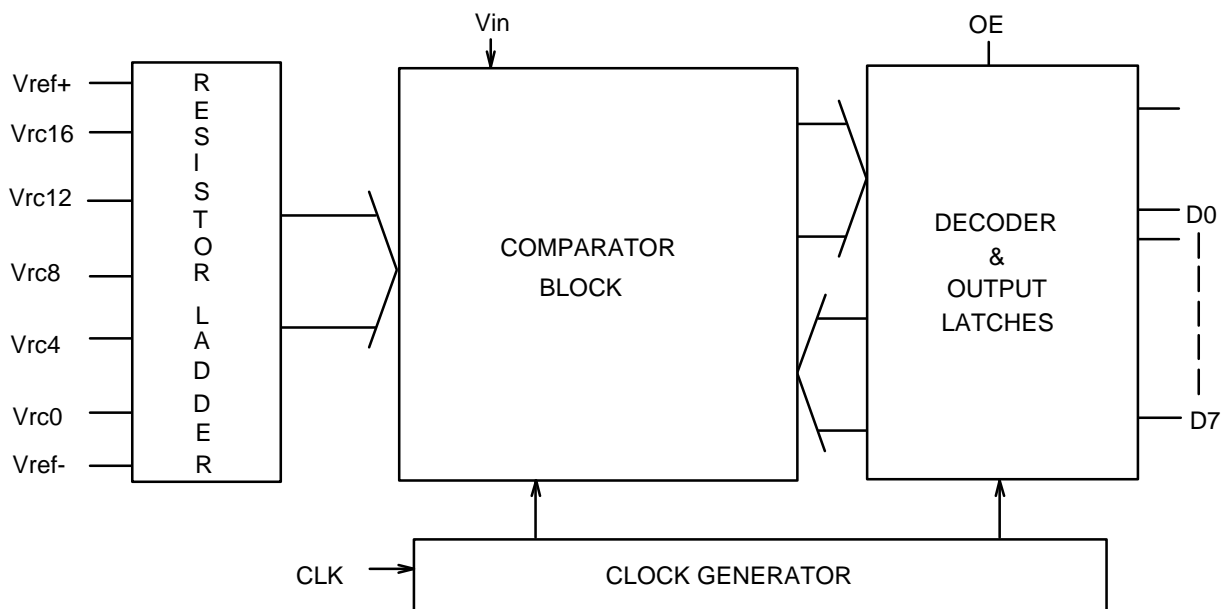
the remainder of the subtractor and after the complete binary code is latched and buffered in the output latches block. To reduce silicon area, a single multiplexed flash converter performs the coarse and the fine conversions.

This cell was designed in two symmetrical banks corresponding to two 10MHz half-flash ADC operating in a ping-pong arrangement. For some applications only one bank may be enough and therefore the cell is divided by two.

Features

- Operating supply voltage 5V
- Supply current 31mA
- Resolution 8 bits
- Linearity error $\pm 0.5\text{LSB}$
- Conversion rate 200M sample/s
- Full scale range (min) 1V
- Exceptionally small silicon area

Functional Block Diagram



HIGH RESOLUTION ADC

Description

A basic cyclic converter can achieve a limited resolution due to the inaccuracy of the times-2 multiplier, the sample/hold feedthrough, and the amplifier gain used in its construction. This minor ACSC function is a high-resolution converter which removes these inaccuracies while still using the sequential conversion technique of any cyclic converter. Thus the rate of conversion is determined by the required resolution and the settling time but, now, conversion can be made to exceed 12 bits with 1LSB integral non-linearity.

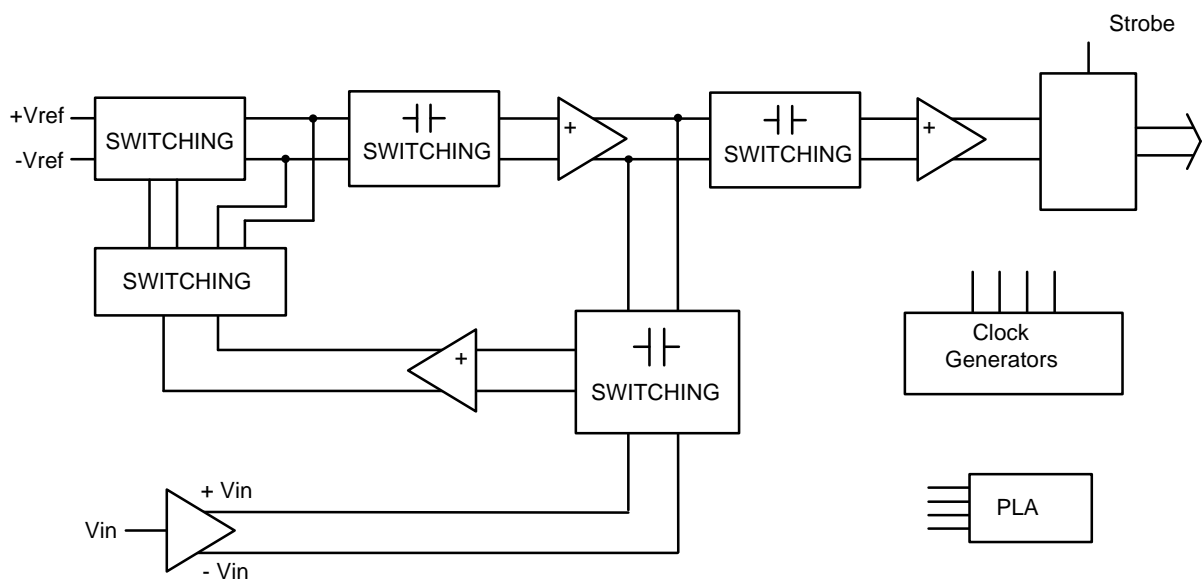
The reference voltage (initially set equal to the MSB) is rotated around the converter loop, interleaved with the

normal cyclic conversion algorithm. This causes the reference voltage to be subjected to the same converter loop tolerances (identified above) as the processed signal. This also relaxes the tolerance and size of the capacitors. Each bit of conversion must take 8 clock cycles in this converter and so the 12 bits requires 96 clock cycles in total. The structure used on this chip employs differential circuitry throughout and the capacitors are switched around the opamps to provide the functions of comparison, subtraction and multiply by -2. The switching and sequencing is provided by an on-chip PLA.

Features

- 12 bits resolution
- Single-chip solution with no external components except crystal oscillator
- For datacomms, telecoms and avionic control applications
- Conversion rate of greater than 10KHz
- +/-5V supply
- No "calibrate cycle" required
- Built in sample/hold
- Low power consumption (15mW)

Functional Block Diagram



BAND-GAP REFERENCE

Description

This minor ACSC function is a 1.2 μ m CMOS Band-gap reference cell for use as an on-chip voltage reference.

The cell uses vertical pnp transistors in the band-gap cell to reduce output voltage spread. A low offset and

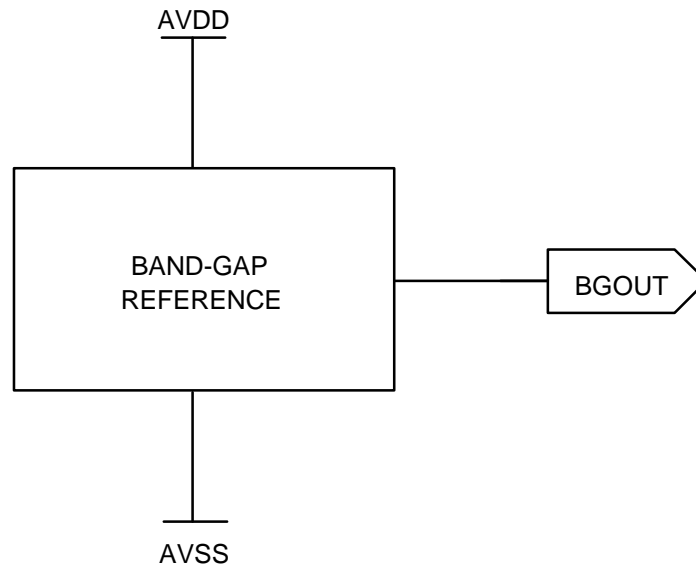
low noise bipolar amplifier is used to provide the loop gain.

The cell has an output impedance of 5K ohm so the output should be buffered for load currents exceeding 10 μ A.

Features

- 1.24 Volt reference +/-4%.
- Supply voltage range 2.5V to 6V
- Temperature coefficient < 100 ppm/ $^{\circ}$ C
- Power supply rejection ratio of >60dB
- Undecoupled output noise < 500 μ V r.m.s.

Functional Block Diagram



HARD LIMITER

Description

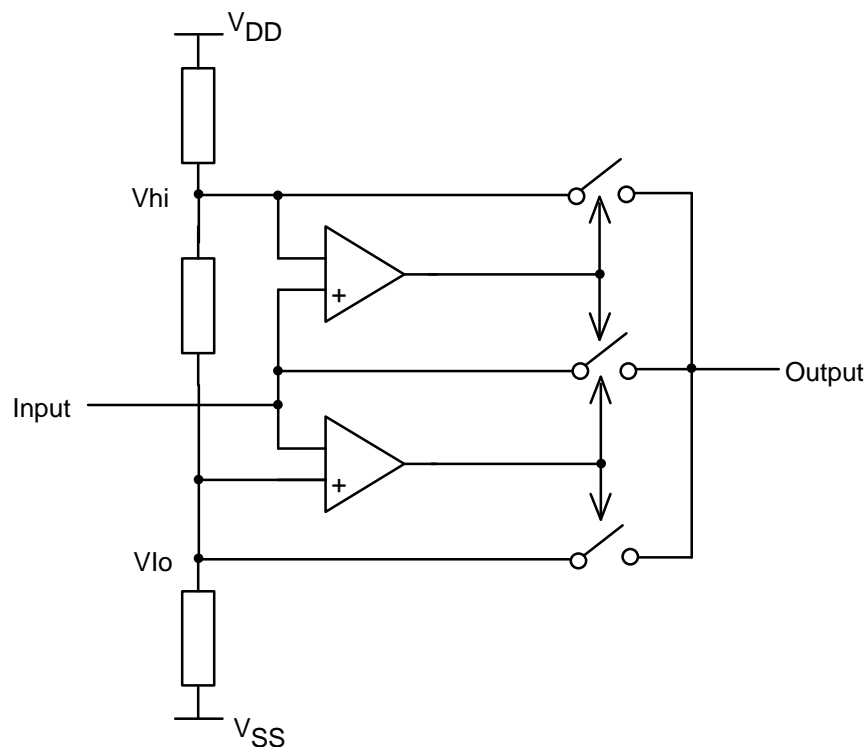
This minor ACSC function is a limiter consisting of two comparators and three switches that clamp the output to the high and low limiting voltages. This type of circuit operates with signals from DC to audio

frequencies. The speed of the comparator will determine the upper frequency response of the limiter. The reference voltages can either be generated as a ratio of the supply voltages, as shown, or derived from a known reference, for example a bandgap.

Features

- Operates from DC to audio frequencies
- Limiting levels set by resistor ratio

Functional Block Diagram



SOFT LIMITER

Description

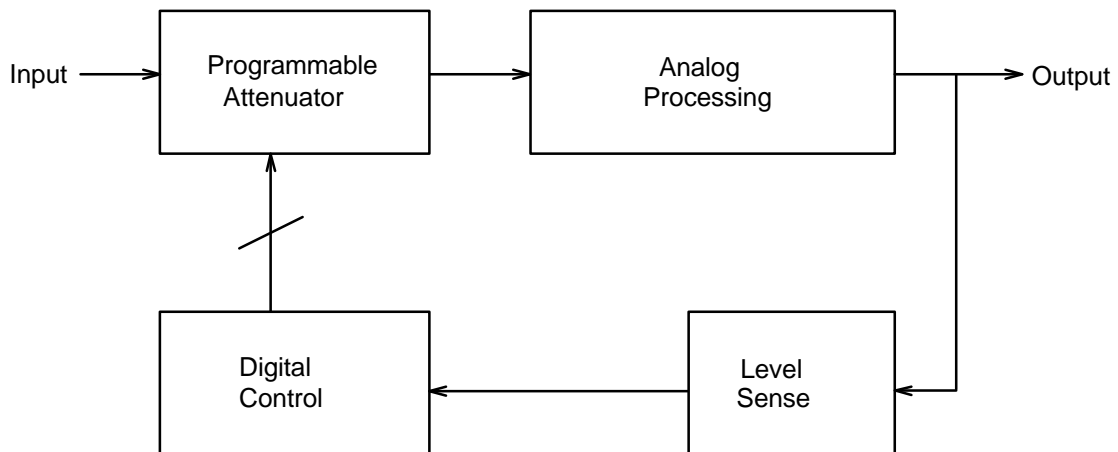
This minor ACSC function is a soft limiter consisting of a gain stage, level sense and digital controller in a closed loop. The signal amplitude is controlled using a digitally programmable attenuation stage driven from an up/down counter. The attack and decay rates are

set in the up/down count speed. The level sensing occurs after any system signal processing (for example filtering) and causes the digital control to count up when the preset limit is exceeded.

Features

- Attack/decay time set in digital controller
- Level sensing requires only a simple comparator
- Preset limit for the sense can easily be made ratiometric with supply voltage

Functional Block Diagram



CLOCK SQUARER

Description

This minor ACSC function is a clock squarer consisting of a fast comparator nested within an integrator loop. The loop provides a slow time-averaged dc threshold for the comparator.

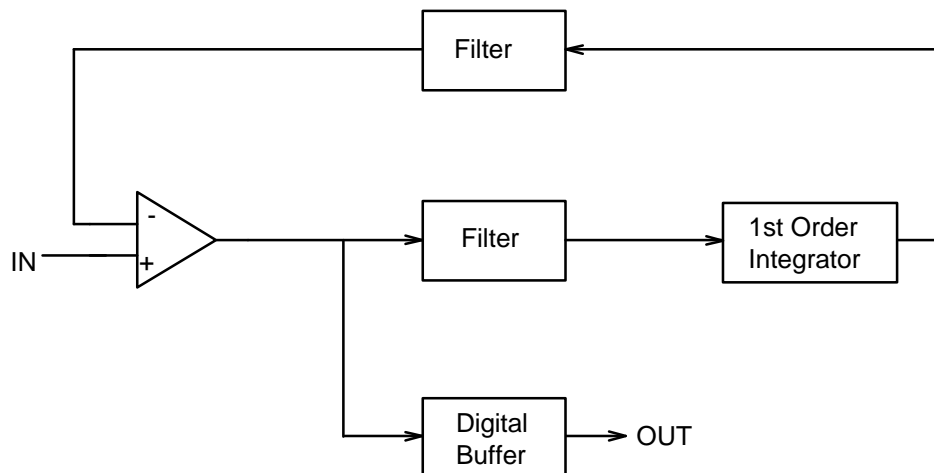
A 1% accurate 50-50 duty cycle square wave, at up to 20MHz, is produced for signal levels as low as 400mVpp within a 2V dc range.

Time constant of integrator loop $\approx 10\mu\text{s}$.
Quiescent supply current approximately 400 μA .

Features

- Provides stable clock with 50-50 duty cycle from a low-level distorted sine/square input
- Internal dc tracking of input signal
- Operation up to 20MHz

Functional Block Diagram



FULL WAVE RECTIFIER

Description

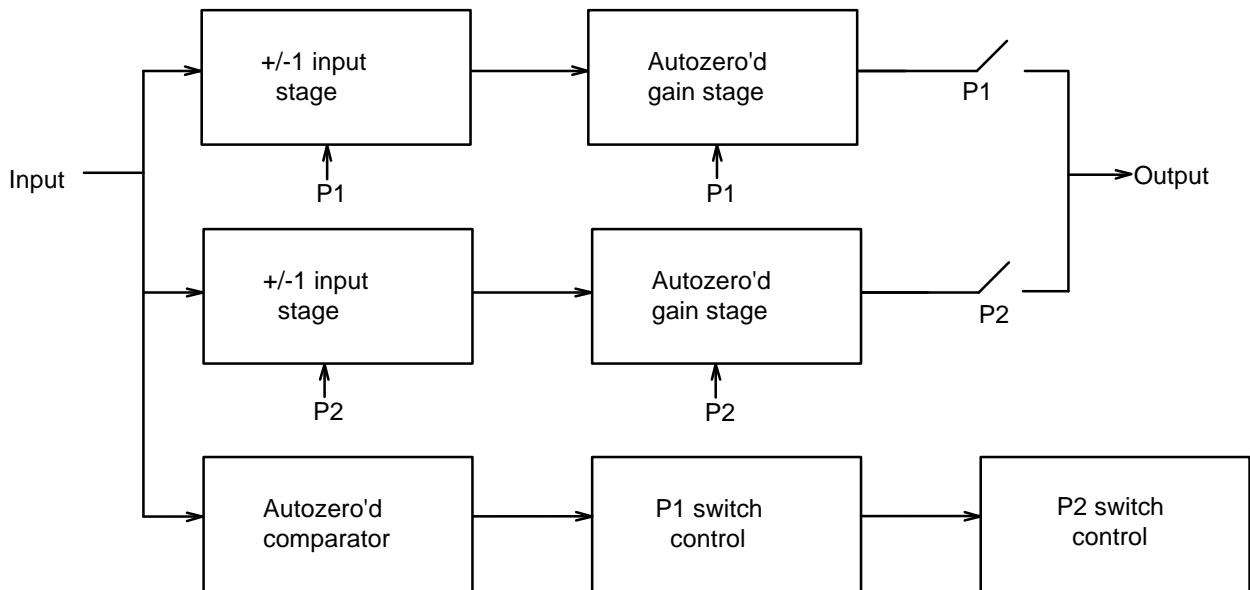
This minor ACSC function is a full wave rectifier, built using two interleaved rectifiers to generate a continuous output. Each rectifier consists of a +/-1 gain stage followed by an autozero'd switched capacitor gain stage. This cancels any amplifier input offset and gives an accurate gain (due to the matching of the capacitor ratio).

The polarity of the input is sensed using an autozero'd comparator that drives the P1 and P2 switch control circuits.

Features

- Low input offset circuit
- Continuous output
- Accurate gain due to SC structure

Functional Block Diagram



MANCHESTER ENCODER

Description

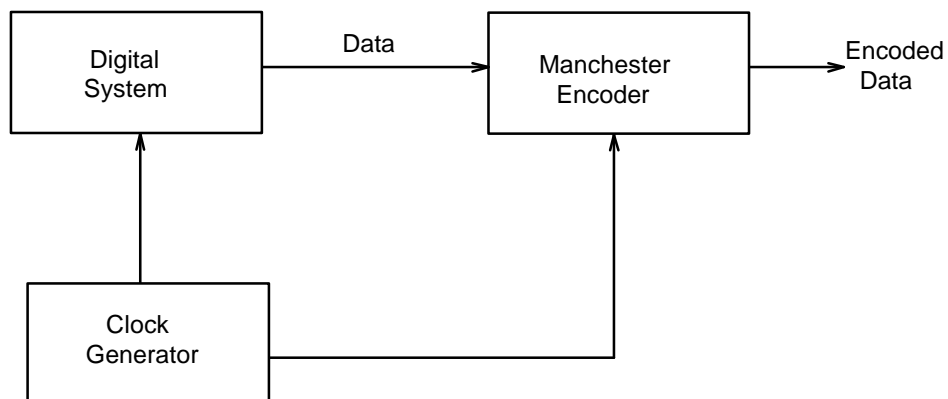
This minor ACSC function provides Manchester coding or digital biphas coding which is used in many applications, for example in Ethernet local area networks. The attraction of this type of coding of the data is that it contains a strong timing component and

zero DC spectral content. In digital biphas coding, one cycle of a square wave with a particular phase is used to indicate a 0. Since there is a transition at the centre of every symbol interval a strong timing signal is available for synchronisation.

Features

- Data contains timing information
- Simple implementation

Functional Block Diagram



BATTERY VOLTAGE DETECTOR

Description

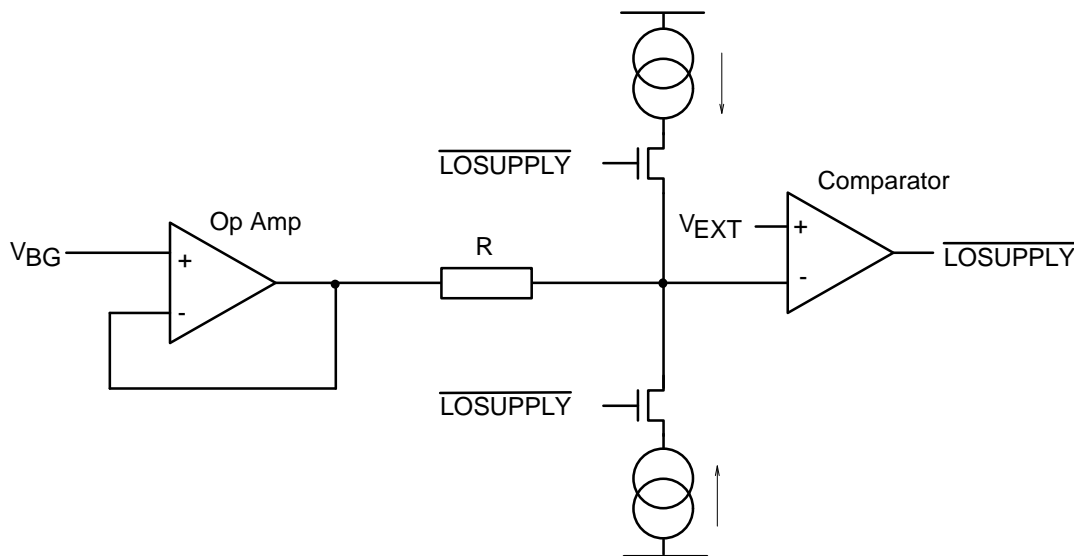
This minor ACSC function is a battery voltage monitor where a buffered bandgap reference voltage is compared to an external voltage, and output LOSUPPLY goes low when $V_{EXT} < V_{TRIP}$. The use of the bandgap reference voltage allows an accurate and temperature stable threshold to be defined.

The positive trip level, as V_{EXT} falls towards V_{BG} , is $V_{BG} - IR$. When $V_{EXT} < V_{BG} - IR$, LOSUPPLY goes low, moving V_{TRIP} to $V_{BG} + IR$. Appropriate choice of I and R allows any noise on V_{EXT} to be rejected, and not cause false triggering of LOSUPPLY.

Features

- Comparator and bandgap reference voltage allows accurate voltage detection
- Incorporates hysteresis to prevent false triggering and output glitches
- Use of external potentiometer allows voltages outside of the supply range of the device to be monitored
- Useful in low battery voltage detection circuits

Functional Block Diagram



VOLTAGE REGULATOR

Description

This minor ACSC function is a 5V voltage regulator and requires just 1 resistor, 1 diode, 1 npn transistor and 1 capacitor to function. It is capable of providing up to 12mA at 5V. The output is accurate to 10% over the temperature range 0-70°C and for input voltages between 6V and 16V.

Features

- 6-16V input voltage range
- 5V \pm 10% output voltage
- 12mA current capability
- Uses just 4 external components

Functional Block Diagram

